## Index of /ds/LM/

	Name	Last modified	Size	Description
1	Parent Directory			
	LM101A.pdf	22-Dec-99 00:11	65K	
	LM101A_LH2101A.pdf	24-Nov-98 00:00	65K	
<u> </u>	LM108A.pdf	22-Dec-99 00:11	59K	
<u>L</u>	LM111.pdf	22-Dec-99 00:11	71K	
<u> </u>	LM124.pdf	22-Dec-99 00:11	68K	
<u> </u>	LM139.pdf	22-Dec-99 00:11	85K	
<u> </u>	LM139A.pdf	22-Dec-99 00:11	85K	
	LM1458.pdf	22-Dec-99 00:11	97K	
	LM1458A.pdf	22-Dec-99 00:11	97K	
	LM1458AI.pdf	22-Dec-99 00:11	97K	
	LM1458AIM.pdf	03-Dec-99 15:48	97K	
<u> </u>	LM1458AIN.pdf	03-Dec-99 15:48	97K	
<u> </u>	LM1458AIS.pdf	03-Dec-99 15:48	97K	
<u> </u>	LM1458AM.pdf	03-Dec-99 15:48	97K	
<u> </u>	LM1458AN.pdf	03-Dec-99 15:48	97K	
<u> </u>	LM1458AS.pdf	03-Dec-99 15:48	97K	
<u> </u>	LM1458I.pdf	22-Dec-99 00:11	97K	
<u> </u>	LM1458IM.pdf	03-Dec-99 15:48	97K	
	LM1458IN.pdf	03-Dec-99 15:48	97K	
<u> </u>	LM1458IS.pdf	03-Dec-99 15:48	97K	
<u> </u>	LM1458M.pdf	03-Dec-99 15:48	97K	
	LM1458N.pdf	03-Dec-99 15:48	97K	
	LM1458S.pdf	03-Dec-99 15:48	97K	

<u> </u>	LM148.pdf	22-Dec-99	00:11	98K
	LM1851.pdf	22-Dec-99	00:11	88K
	LM1882.pdf	25-Aug-97	17:20	228K
	LM224.pdf	22-Dec-99	00:11	1M
	LM224A.pdf	22-Dec-99	00:11	1M
	LM236-2.5.pdf	22-Dec-99	00:11	134K
	LM239.pdf	22-Dec-99	00:11	144K
	LM239A.pdf	22-Dec-99	00:11	144K
	LM239AM.pdf	03-Dec-99	15:48	144K
	LM239AN.pdf	03-Dec-99	15:48	144K
	LM239M.pdf	03-Dec-99	15:48	144K
	LM239N.pdf	03-Dec-99	15:48	144K
	LM248.pdf	08-Feb-00	00:00	1M
	LM248M.pdf	22-Dec-99	00:11	1M
	LM248N.pdf	22-Dec-99	00:11	1M
	LM258.pdf	08-Feb-00	00:00	1M
	LM258A.pdf	08-Feb-00	00:00	1M
	LM258AM.pdf	22-Dec-99	00:11	1M
	LM258AN.pdf	22-Dec-99	00:11	1M
	LM258AS.pdf	22-Dec-99	00:11	1M
	LM258M.pdf	22-Dec-99	00:11	1M
	LM258N.pdf	22-Dec-99	00:11	1M
	LM258S.pdf	22-Dec-99	00:11	1M
	LM2901.pdf	22-Dec-99	00:11	144K
	LM2901M.pdf	03-Dec-99	15:48	144K
	LM2901N.pdf	03-Dec-99	15:48	144K
	LM2902.pdf	22-Dec-99	00:11	1M

LÌ.	LM2903.pdf	08-Feb-00	00:00	119K
	LM2903M.pdf	03-Dec-99	15:48	169K
	LM2903N.pdf	03-Dec-99	15:48	169K
	LM2903S.pdf	03-Dec-99	15:48	169K
	LM2904.pdf	08-Feb-00	00:00	1M
	LM2904M.pdf	22-Dec-99	00:11	1M
	LM2904N.pdf	22-Dec-99	00:11	1M
	LM2904S.pdf	22-Dec-99	00:11	1M
	LM293.pdf	08-Feb-00	00:00	119K
	LM293A.pdf	08-Feb-00	00:00	119K
	LM293AM.pdf	03-Dec-99	15:48	169K
	LM293AN.pdf	03-Dec-99	15:48	169K
	LM293AS.pdf	03-Dec-99	15:48	169K
	LM293M.pdf	03-Dec-99	15:48	169K
	LM293N.pdf	03-Dec-99	15:48	169K
	LM293S.pdf	03-Dec-99	15:48	169K
	LM311.pdf	22-Dec-99	00:11	427K
	LM311M.pdf	03-Dec-99	15:48	427K
	LM311N.pdf	03-Dec-99	15:48	427K
	LM317L.pdf	22-Dec-99	00:11	156K
	LM324.pdf	17-Feb-00	00:00	68K
	LM324A.pdf	22-Dec-99	00:11	1M
	LM3301.pdf	22-Dec-99	00:11	144K
	LM3301M.pdf	03-Dec-99	15:48	144K
	LM3301N.pdf	03-Dec-99	15:48	144K
	LM336-2.5.pdf	22-Dec-99	00:11	134K
	LM336-2.5B.pdf	22-Dec-99	00:11	134K

<del>_</del> .				
<u>L</u> ì_	LM337.pdf	22-Dec-99	00:11	51K
	LM339.pdf	17-Feb-00	00:00	85K
	LM339A.pdf	22-Dec-99	00:11	144K
	LM339AM.pdf	03-Dec-99	15:48	144K
	LM339AN.pdf	03-Dec-99	15:48	144K
	LM339M.pdf	03-Dec-99	15:48	144K
	LM339N.pdf	03-Dec-99	15:48	144K
	LM348.pdf	08-Feb-00	00:00	1M
	LM348M.pdf	22-Dec-99	00:11	1M
	LM348N.pdf	22-Dec-99	00:11	1M
	LM353.pdf	22-Dec-99	00:11	49K
	LM358.pdf	08-Feb-00	00:00	1M
	LM358A.pdf	08-Feb-00	00:00	1M
	LM358AM.pdf	22-Dec-99	00:11	1M
	LM358AN.pdf	22-Dec-99	00:11	1M
	LM358AS.pdf	22-Dec-99	00:11	1M
	LM358M.pdf	22-Dec-99	00:11	1M
	LM358N.pdf	22-Dec-99	00:11	1M
	LM358S.pdf	22-Dec-99	00:11	1M
	LM393.pdf	08-Feb-00	00:00	119K
	LM393A.pdf	08-Feb-00	00:00	119K
	LM393AM.pdf	03-Dec-99	15:48	169K
	LM393AN.pdf	03-Dec-99	15:48	169K
	LM393AS.pdf	03-Dec-99	15:48	169K
	LM393M.pdf	03-Dec-99	15:48	169K
	LM393N.pdf	03-Dec-99	15:48	169K
Lì_	LM393S.pdf	03-Dec-99	15:48	169K

- N				
<u> </u>	LM442.pdf	22-Dec-99	00:11	53K
<u> </u>	LM442AN.pdf	22-Dec-99	00:11	53K
	LM442AS.pdf	22-Dec-99	00:11	53K
	LM442N.pdf	22-Dec-99	00:11	53K
	LM442S.pdf	22-Dec-99	00:11	53K
	LM555.pdf	08-Feb-00	00:00	82K
	LM555I.pdf	08-Feb-00	00:00	82K
	LM555IM.pdf	22-Dec-99	00:11	82K
	LM555IN.pdf	22-Dec-99	00:11	82K
<u> </u>	LM555M.pdf	22-Dec-99	00:11	82K
<u> </u>	LM555N.pdf	22-Dec-99	00:11	82K
	LM556.pdf	22-Dec-99	00:11	59K
<u> </u>	LM710.pdf	22-Dec-99	00:11	159K
<u> </u>	LM710I.pdf	22-Dec-99	00:11	159K
<u> </u>	LM710IM.pdf	22-Dec-99	00:11	159K
	LM710IN.pdf	22-Dec-99	00:11	159K
<u>L</u>	LM710M.pdf	22-Dec-99	00:11	159K
<u> </u>	LM710N.pdf	22-Dec-99	00:11	159K
	LM711.pdf	22-Dec-99	00:11	69K
<u> </u>	LM711I.pdf	22-Dec-99	00:11	69K
	LM711IM.pdf	22-Dec-99	00:11	69K
<u>[</u> ]_	LM711IN.pdf	22-Dec-99	00:11	69K
<u> </u>	LM711M.pdf	22-Dec-99	00:11	69K
<u> </u>	LM711N.pdf	22-Dec-99	00:11	69K
	LM741.pdf	08-Feb-00	00:00	986K
<u> </u>	LM741E.pdf	08-Feb-00	00:00	986K
Lì_	LM741EI.pdf	08-Feb-00	00:00	986K

<u>—</u> .				
	LM741EIM.pdf	22-Dec-99	00:12	986K
	LM741EIN.pdf	22-Dec-99	00:12	986K
	LM741EM.pdf	22-Dec-99	00:12	986K
	LM741EN.pdf	22-Dec-99	00:12	986K
	LM741I.pdf	08-Feb-00	00:00	986K
	LM741IM.pdf	22-Dec-99	00:12	986K
<u> </u>	LM741IN.pdf	22-Dec-99	00:12	986K
	LM741M.pdf	22-Dec-99	00:12	986K
	LM741N.pdf	22-Dec-99	00:12	986K
	LM7805.pdf	22-Dec-99	00:12	516K
	LM7805A.pdf	16-Apr-99	00:00	516K
	LM7806.pdf	22-Dec-99	00:12	516K
	LM7806A.pdf	16-Apr-99	00:00	516K
	LM7808.pdf	22-Dec-99	00:12	516K
	LM7808A.pdf	16-Apr-99	00:00	516K
	LM7809.pdf	22-Dec-99	00:12	516K
<u> </u>	LM7809A.pdf	16-Apr-99	00:00	516K
<u> </u>	LM7810.pdf	22-Dec-99	00:12	516K
	LM7810A.pdf	16-Apr-99	00:00	516K
	LM7811.pdf	22-Dec-99	00:12	516K
	LM7811A.pdf	16-Apr-99	00:00	516K
<u> </u>	LM7812.pdf	22-Dec-99	00:12	516K
	LM7812A.pdf	16-Apr-99	00:00	516K
<u> </u>	LM7815.pdf	22-Dec-99	00:12	516K
	LM7815A.pdf	16-Apr-99	00:00	516K
	LM7818.pdf	22-Dec-99	00:12	516K
<u> </u>	LM7818A.pdf	16-Apr-99	00:00	516K

<u>[</u> ]_	LM7824.pdf	22-Dec-99	00:12	516K
	LM7824A.pdf	16-Apr-99	00:00	516K
	LM78L05.pdf	22-Dec-99	00:12	118K
	LM78L06.pdf	22-Dec-99	00:12	118K
	LM78L08.pdf	22-Dec-99	00:12	118K
<u> </u>	LM78L09.pdf	22-Dec-99	00:12	118K
<u> </u>	LM78L10.pdf	22-Dec-99	00:12	118K
	LM78L12.pdf	22-Dec-99	00:12	118K
<u> </u>	LM78L15.pdf	22-Dec-99	00:12	118K
	LM78L18.pdf	22-Dec-99	00:12	118K
	LM78L24.pdf	22-Dec-99	00:12	118K
	LM78LXX.pdf	22-Dec-99	00:12	118K
	LM78M05.pdf	08-Feb-00	00:00	136K
	LM78M06.pdf	16-Apr-99	00:00	159K
	LM78M08.pdf	08-Feb-00	00:00	136K
	LM78M10.pdf	08-Feb-00	00:00	136K
<u>_</u>	LM78M12.pdf	08-Feb-00	00:00	136K
<u>[</u> ]_	LM78M15.pdf	08-Feb-00	00:00	136K
	LM78M18.pdf	08-Feb-00	00:00	136K
	LM78M20.pdf	08-Feb-00	00:00	136K
	LM78M24.pdf	08-Feb-00	00:00	136K
<u>[</u> ]_	LM78MXX.pdf	08-Feb-00	00:00	136K
	LM78XX.pdf	22-Dec-99	00:12	516K
	LM7905.pdf	22-Dec-99	00:12	194K
<u>L</u>	LM7905A.pdf	22-Dec-99	00:12	194K
<u>[</u> ]_	LM7906.pdf	22-Dec-99	00:12	194K
<u> </u>	LM7906A.pdf	22-Dec-99	00:12	194K

_				
<u>L</u>	LM7908.pdf	22-Dec-99	00:12	194K
<u> </u>	LM7908A.pdf	22-Dec-99	00:12	194K
	LM7909.pdf	16-Apr-99	00:00	194K
	LM7912.pdf	22-Dec-99	00:12	194K
	LM7912A.pdf	22-Dec-99	00:12	194K
	LM7915.pdf	22-Dec-99	00:12	194K
	LM7915A.pdf	22-Dec-99	00:12	194K
	LM7918.pdf	22-Dec-99	00:12	194K
	LM7918A.pdf	22-Dec-99	00:12	194K
	LM7924.pdf	22-Dec-99	00:12	194K
	LM7924A.pdf	22-Dec-99	00:12	194K
	LM79L05A.pdf	08-Feb-00	00:00	389K
	LM79L12A.pdf	08-Feb-00	00:00	389K
	LM79L15A.pdf	08-Feb-00	00:00	389K
	LM79L18A.pdf	08-Feb-00	00:00	389K
	LM79L24A.pdf	08-Feb-00	00:00	389K
	LM79LXXA.pdf	08-Feb-00	00:00	389K
	LM79M05.pdf	16-Apr-99	00:00	113K
	LM79M06.pdf	16-Apr-99	00:00	113K
	LM79M08.pdf	16-Apr-99	00:00	113K
	LM79M12.pdf	16-Apr-99	00:00	113K
	LM79M15.pdf	16-Apr-99	00:00	113K
	LM79M18.pdf	16-Apr-99	00:00	113K
<u> </u>	LM79M24.pdf	16-Apr-99	00:00	113K
	LM79MXX.pdf	08-Feb-00	00:00	254K
	LM79XX.pdf	22-Dec-99	00:12	194K
Lì_	LM79XXA.pdf	22-Dec-99	00:12	194K



## LM101A/LH2101A

## **General Purpose Operational Amplifier**

#### **Features**

- Input offset voltage 0.7 mV
- Input bias current 30 nA
- Input offset current 1.5 nA
- Full frequency compensation 30pF
- Supply voltage  $\pm 5.0$ V to  $\pm 20$ V

## **Description**

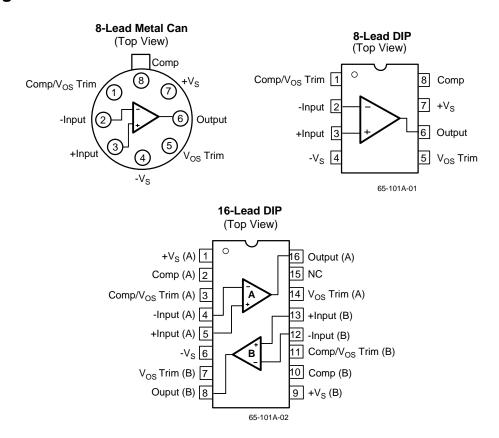
The LM101A/LH2101A is a general purpose high performance operational amplifier fabricated monolithically on a silicon chip by an advanced epitaxial process. The LH2101A consists of two LM101A ICs in one 16-lead DIP. The units may be fully compensated with the addition of a 30 pF capacitor stabilizing the circuit for all feedback configurations including capacitive loads.

The device may be operated as a comparator with a differential input as high as 30V. Used as a comparator the output can be clamped at any desired level to make it compatible with logic circuits.

The LM101A and LH2101A operate over the full military temperature range from -55°C to +125°C.

LM101A/LH2101A PRODUCT SPECIFICATION

## **Pin Assignments**



## **Absolute Maximum Ratings**

Parameter	Min.	Max.	Units
Supply Voltage		±22	V
Differential Input Voltage		30	V
Input Voltage <sup>1</sup>		±15	V
Output Short-Circuit Duration <sup>2</sup>	Indefinite		
Storage Temperature Range	-65	+150	°C
Operating Temperature Range	-55	+125	°C
Lead Soldering Temperature (60 sec)		+300	°C

- 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
- 2. Observe package thermal characteristics.

## **Thermal Characteristics**

Parameter	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	16-Lead Ceramic DIP
Maximum Junction Temperature	+175°C	+175°C	+175°C
Maximum P <sub>D</sub> T <sub>A</sub> <50°C	833 mW	658 mW	1042 mW
Thermal Resistance, θ <sub>JC</sub>	45°C/W	50°C/W	60°C/W
Thermal Resistance, θJA	150°C/W	190°C/W	120°C/W
For T <sub>A</sub> > 50°C Derate at	8.33 mW/°C	5.26 mW/°C	8.33 mW/°C

## **Electrical Characteristics**

C = 30pF;  $\pm 5.0$ V  $\leq$  VS  $\leq$   $\pm 20$ V; -55°C  $\leq$  TA  $\leq$  +125°C unless otherwise specified

		LM101A/LH2101 A			
Parameters	Test Conditions	MIn.	Тур.	Max.	Units
Input Offset Voltage	$T_A = +25^{\circ}C$ , $R_S \le 50 \text{ k}\Omega$		0.7	2.0	mV
Input Offset Current	T <sub>A</sub> = +25°C		1.5	10	nA
Input Bias Current	T <sub>A</sub> = +25°C		30	75	nA
Input Resistance	T <sub>A</sub> = +25°C	1.5	4.0		MΩ
Supply Current	TA = +25°C VS = ±20V		1.8	3.0	mA
Large Signal Voltage Gain	$T_A = +25^{\circ}C$ , $V_S = \pm 15V$ $V_{OUT} = \pm 10V$ , $R_L \ge 2$ $K\Omega$	50	160		V/mV
Input Offset Voltage	Rs ≤ 50 KΩ			3.0	mV
Average Input Offset Voltage Drift	R <sub>S</sub> ≤ 50 KΩ		3.0	15	μV/°C
Input Offset Current				20	nA
Average Input Offset Current Drift	+25°C ≤ T <sub>A</sub> +125°C		0.01	0.1	nA/°C
	-55°C ≤ TA +25°C		0.02	0.2	
Input Bias Current				100	nA
Supply Current	T <sub>A</sub> = +125°C, V <sub>S</sub> = ±20V		1.2	2.5	mA
Large Signal Voltage Gain	$V_S = \pm 15V$ $V_{OUT} = \pm 10V$ , $R_L \ge 2$ KΩ	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$ , $R_L = 10 \text{ K}\Omega$	±12	±14		V
	R <sub>L</sub> = 2 KΩ	±10	±13		1
Input Voltage Range	Vs = ±20V	±15			V
Common Mode Rejection Ratio	Rs ≤ 50 KΩ	80	96		dB
Power Supply Rejection Ratio	R <sub>S</sub> ≤ 50 KΩ	80	96		dB

LM101A/LH2101A PRODUCT SPECIFICATION

## **Typical Performance Characteristics**

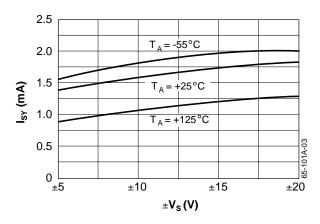


Figure 1. Supply Current vs. Supply Voltage

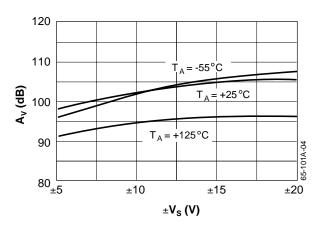


Figure 2. Voltage Gain vs. Supply Voltage

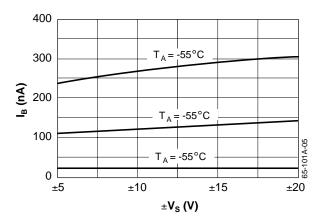


Figure 3. Input Bias Current vs. Supply Voltage

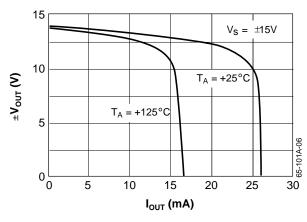


Figure 4. Current Limiting Output Voltage vs. Output Current

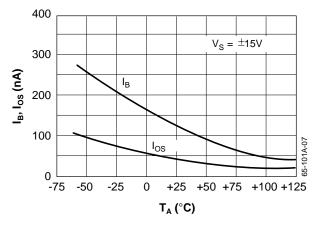


Figure 5. Input Bias, Offset Current vs. Temperature

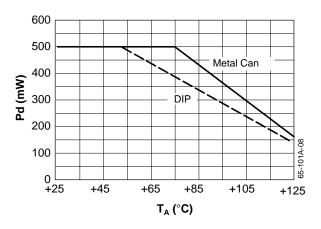
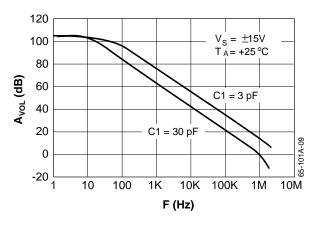


Figure 6. Maximum Power Dissipation vs. Temperature

## **Typical Performance Characteristics** (continued)



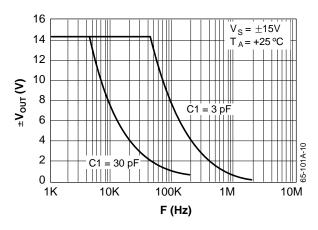


Figure 7. Open Loop Gain vs. Frequency

Figure 8. Output Voltage Swing vs. Frequency

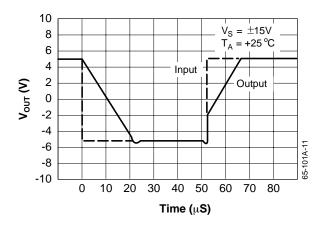
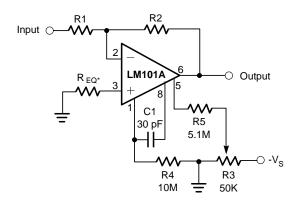


Figure 9. Follower Large Signal Pulse Response Output Voltage vs. Time

LM101A/LH2101A PRODUCT SPECIFICATION

## **Typical Applications**



\*May be zero or equal to parallel combination of R1 and R2 for minimum offset.

65-101A-12

Figure 10. Inverting Amplifier with Balancing Circuit

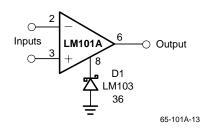


Figure 11. Voltage Comparator for Driving DTL or TTL ICs

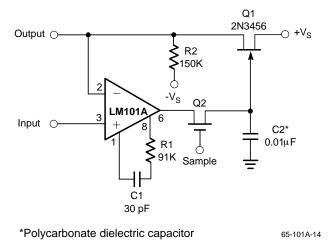


Figure 12. Low Drift Sample and Hold

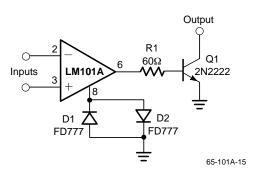
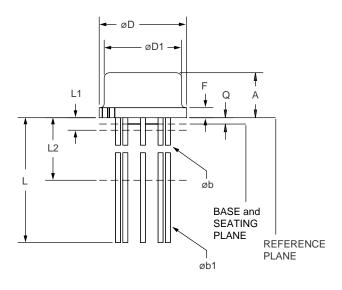


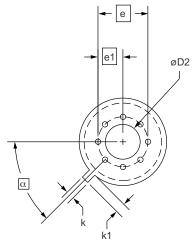
Figure 13. Voltage Comparator for Driving RTL Logic or High Current Driver

LM101A/LH2101A PRODUCT SPECIFICATION

#### **Mechanical Dimensions**

#### 8-Lead TO-99 Metal Can





Symbol	Inc	hes	Millimeters		Notes
Symbol	Min.	Max.	Min.	Max.	Notes
Α	.165	.185	4.19	4.70	
øb	.016	.019	.41	.48	1, 5
øb1	.016	.021	.41	.53	1, 5
øD	.335	.375	8.51	9.52	
øD1	.305	.335	7.75	8.51	
øD2	.110	.160	2.79	4.06	
е	.200	BSC	5.08	5.08 BSC	
e1	.100	BSC	2.54	BSC	
F		.040	_	1.02	
k	.027	.034	.69	.86	
k1	.027	.045	.69	1.14	2
L	.500	.750	12.70	19.05	1
L1	_	.050	_	1.27	1
L2	.250	_	6.35	_	1
Q	.010	.045	.25	1.14	
α	45°	BSC	45°	BSC	

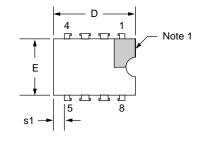
- (All leads) øb applies between L1 & L2. øb1 applies between L2 & .500 (12.70mm) from the reference plane. Diameter is uncontrolled in L1 & beyond .500 (12.70mm) from the reference plane.
- 2. Measured from the maximum diameter of the product.
- 3. Leads having a maximum diameter .019 (.48mm) measured in gauging plane, .054 (1.37mm) +.001 (.03mm) -.000 (.00mm) below the reference plane of the product shall be within .007 (.18mm) of their true position relative to a maximum width tab
- 4. The product may be measured by direct methods or by gauge.
- 5. All leads increase maximum limit by .003 (.08mm) when lead finish is applied.

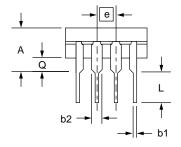
LM101A/LH2101A PRODUCT SPECIFICATION

## **Mechanical Dimensions** (continued)

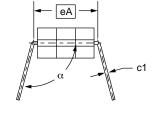
#### 8-Lead Ceramic DIP

Symbol	Inc	hes	Millimeters		Notes	
Syllibol	Min.	Max.	Min.	Max.	Notes	
Α	_	.200	_	5.08		
b1	.014	.023	.36	.58	8	
b2	.045	.065	1.14	1.65	2, 8	
c1	.008	.015	.20	.38	8	
D	_	.405	_	10.29	4	
Е	.220	.310	5.59	7.87	4	
е	.100	BSC	2.54	BSC	5, 9	
eA	.300	BSC	7.62	BSC	7	
L	.125	.200	3.18	5.08		
Ø	.015	.060	.38	1.52	3	
s1	.005	_	.13	_	6	
α	90°	105°	90°	105°		





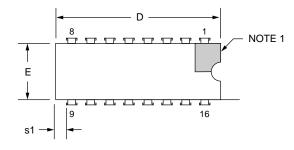
- Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
- 2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
- 3. Dimension "Q" shall be measured from the seating plane to the base plane.
- 4. This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
- 6. Applies to all four corners (leads number 1, 4, 5, and 8).
- 7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when " $\alpha$ " is  $90^\circ.$
- 8. All leads Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
- 9. Six spaces.

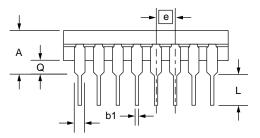


## **Mechanical Dimensions** (continued)

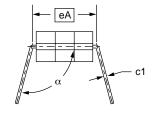
#### 16-Lead Ceramic DIP

Comple at	Inc	hes	Millimeters		Notes
Symbol	Min.	Max.	Min.	Max.	Notes
Α	_	.200	_	5.08	
b1	.014	.023	.36	.58	8
b2	.050	.065	1.27	1.65	2
c1	.008	.015	.20	.38	8
D	.745	.840	18.92	21.33	4
Е	.220	.310	5.59	7.87	4
е	.100	.100 BSC		BSC	5, 9
eA	.300	BSC	7.62	BSC	7
L	.115	.160	2.92	4.06	
Q	.015	.060	.38	1.52	3
s1	.005	_	.13	_	6
α	90°	105°	90°	105°	





- Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
- 2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 8, 9 and 16 only.
- 3. Dimension "Q" shall be measured from the seating plane to the base plane.
- 4. This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 16.
- 6. Applies to all four corners (leads number 1, 8, 9, and 16).
- "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "a" is 90°.
- 8. All leads Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
- 9. Fourteen spaces.



## **Ordering Information**

Part Number	Package	Operating Temperature Range
LM101AD	8-Lead Ceramic DIP	-55°C to +125°C
LM101AD/883B	8-Lead Ceramic DIP	-55°C to +125°C
LM101AT	8-Lead Metal Can	-55°C to +125°C
LM101AT/883B	8-Lead Metal Can	-55°C to +125°C
LH2101AD	16-Lead Ceramic DIP	-55°C to +1 25°C
LH2101AD/883B	16-Lead Ceramic DIP	-55°C to +125°C

#### Notes:

- 1. /883B suffix denotes Mil-Std-883. Level B processing.
- 2. Contact a Fairchild Semiconductor sales office or representative for ordering information on special package/ temperature range combinations.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com



## LM108A/LH2108A

## **Precision Operational Amplifiers**

#### **Features**

- Low input bias current 2 nA
- Low input offset current 200 pA
- Low input offset voltage 500μV
- Low input offset drift  $5 \mu V/^{\circ}C$
- Wide supply range ±3V to ±20V
- Low supply current 0.6 mA
- High PSRR 96 dB
- High CMRR 96 dB
- MIL-STD-883B available

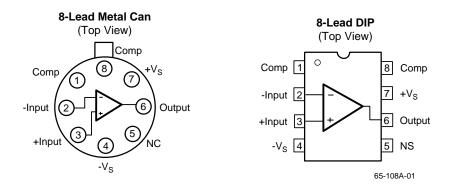
## **Description**

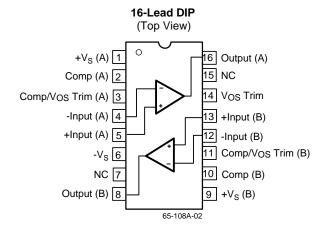
The LM108A operational amplifiers features low input bias current combined with the advantages of bipolar transistor construction; input offset voltages and currents are kept low over a wide range of temperature and supply voltage. Fairchild Semiconductor's superbeta bipolar manufacturing process includes extra treatment at epitaxial growth to ensure low input voltage noise.

The LH2108 consists of two LM108 ICs in one 16-lead DIP. The "A" versions meet tighter electrical specifications than the plain versions. All types are available with 883B military screening.

LM108A/LH2108A PRODUCT SPECIFICATION

## **Pin Assignments**





## **Absolute Maximum Ratings**

Parameter	Min.	Max.	Units
Supply Voltage		±20	V
Differential Input Current <sup>1</sup>		±10	mA
Input Voltage <sup>2</sup>		±15	V
Output Short-Circuit Duration <sup>2</sup>	Continuous		
Operating Temperature Range	-55	+125	°C
Storage Temperature Range	-65	+150	°C
Lead Soldering Temperature (60 seconds)		+300	°C

- 1. The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, if a differential input voltage in excess of 1V is applied between the inputs, excessive current will flow, unless some limiting resistance is provided.
- 2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

## **Thermal Characteristics**

Parameter	8-Lead Metal Can	8-Lead Ceramic DIP	16-Lead Ceramic DIP
Maximum Junction Temperature	+175°C	+175°C	+175°C
Max. P <sub>D</sub> T <sub>A</sub> < 50°C	658 mW	833 mW	1042 mW
Thermal Resistance, θJC	50°C/W	45°C/W	60°C/W
Thermal Resistance, θ <sub>JA</sub>	190°C/W	150°C/W	120°C/W
For T <sub>A</sub> > 50°C Derate at	5.26 mW/°C	8.33 mW/°C	8.38 mW/°C

## **Electrical Characteristics**

 $\pm 5$ V,  $\leq$  VS  $\leq$   $\pm 20$ V and TA  $\leq$  +25°C unless otherwise noted

		LM10	)8A/LH2	108A	LM	108/LH2	108	
Parameters	Test Conditions	Min.	Тур.	Max.	Min.	Тур.	Max.	Units
Input Offset Voltage			0.3	0.5		0.7	2.0	mV
Input Offset Current			0.05	0.2		0.05	0.2	nA
Input Bias Current			0.8	2.0		0.8	2.0	nA
Input Resistance1		30	70		30	70		MΩ
Large Signal Voltage Gain	$V_S = \pm 15V$ , $V_{OUT} \pm 10V$ , $R_L \ge 10K\Omega$	80	300		50	300		V/mV
Supply Current	Each Amplifier		0.3	0.6		0.3	0.6	mA
$\pm 5$ V, $\leq$ VS $\leq$ $\pm 20$ V; $-55$ °C	S ≤ TA ≤ +25°C unless of	herwise r	oted	•			•	•
Input Offset Voltage			0.4	1.0		1.0	3.0	mV
Avg. Input Offset Voltage Drift <sup>2</sup>			1.0	5.0		3.0	15	μV/°C
Input Offset Current			0.1	0.4		0.1	0.4	nA
Avg. Input Offset Current Drift <sup>2</sup>			0.5	2.5		0.5	2.5	pA/°C
Input Bias Current			1.0	3.0		1.0	3.0	nA
Large Signal Voltage Gain	$V_S = \pm 15V$ , $V_{OUT} = \pm 10V$ , $R_L \ge 10 \text{ K}\Omega$	40	200		25	200		V/mV
Output Voltage Swing	R <sub>L</sub> $\ge$ 10 KΩ, V <sub>S</sub> = ±20V	±16	±18		±16	±18		V
Input Voltage Range	Vs = ±15V	±13.5			±13.5			V
Common Mode Rejection Ratio	$VCM = \pm 13.5V,$ $VS = \pm 15V$	96	110		85	100		dB
Power Supply Rejection Ratio	VS = ±15V	96	110		80	96		dB
Supply Current	Each Amplifier			0.6			0.6	mA

- 1. Guaranteed by input bias current specification.
- 2. Sample tested.

LM108A/LH2108A PRODUCT SPECIFICATION

## **Typical Applications**

The LM108 series has very low input offset and bias currents; the user is cautioned that printed circuit board leakages can produce significant errors especially at high board temperatures. Careful attention to board layout and

Figure 1. Offset Adjustment for Non-Inverting Amplifiers

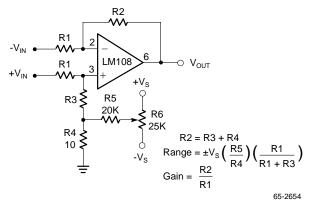


Figure 3. Offset Adjustment for Differential Amplifiers

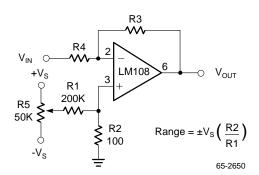


Figure 5. Offset Adjustment for Inverting Amplifiers

cleaning procedure is required to achieve the LM108A's rated performance. It is suggested that board leakage be minimized by encircling the input pins with a guard ring maintained at a potential close to that of the inputs. The guard ring should be driven by a low impedance source such as an amplifier's output or ground.

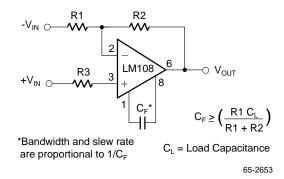
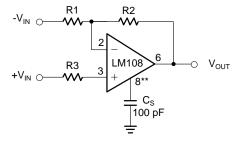


Figure 2. Standard Compensation Circuit



\*Improves rejection of power supply noise by a factor of 10.

65-2655

Figure 4. Alternate Frequency Compensation

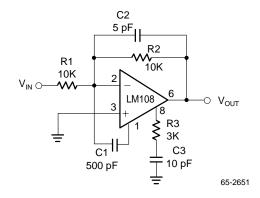
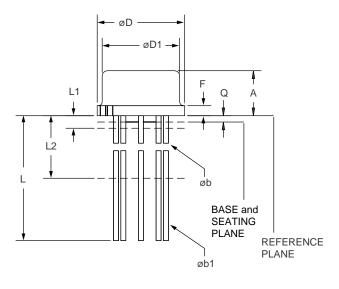


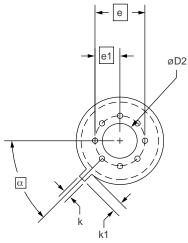
Figure 6. Feedforward Compensation

<sup>\*\*</sup>Bandwidth and slew rate are proportional to 1/C<sub>S</sub>.

#### **Mechanical Dimensions**

#### 8-Lead TO-99 Metal Can





Cumb al	Inc	hes	Millimeters		Notes
Symbol	Min.	Max.	Min.	Max.	Notes
A	.165	.185	4.19	4.70	
øb	.016	.019	.41	.48	1, 5
øb1	.016	.021	.41	.53	1, 5
øD	.335	.375	8.51	9.52	
øD1	.305	.335	7.75	8.51	
øD2	.110	.160	2.79	4.06	
е	.200	BSC	5.08	BSC	
e1	.100	BSC	2.54	BSC	
F	_	.040	_	1.02	
k	.027	.034	.69	.86	
k1	.027	.045	.69	1.14	2
L	.500	.750	12.70	19.05	1
L1	_	.050	_	1.27	1
L2	.250	_	6.35	_	1
Q	.010	.045	.25	1.14	
α	45°	BSC	45°	BSC	

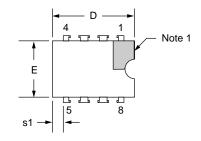
- (All leads) øb applies between L1 & L2. øb1 applies between L2 & .500 (12.70mm) from the reference plane. Diameter is uncontrolled in L1 & beyond .500 (12.70mm) from the reference plane.
- 2. Measured from the maximum diameter of the product.
- 3. Leads having a maximum diameter .019 (.48mm) measured in gauging plane, .054 (1.37mm) +.001 (.03mm) -.000 (.00mm) below the reference plane of the product shall be within .007 (.18mm) of their true position relative to a maximum width tah
- 4. The product may be measured by direct methods or by gauge.
- 5. All leads increase maximum limit by .003 (.08mm) when lead finish is applied.

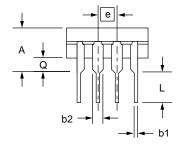
LM108A/LH2108A PRODUCT SPECIFICATION

## **Mechanical Dimensions** (continued)

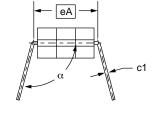
#### 8-Lead Ceramic DIP

Symbol	Inc	hes	Millimeters		Notes	
Symbol	Min.	Max.	Min.	Max.	Notes	
Α	_	.200	_	5.08		
b1	.014	.023	.36	.58	8	
b2	.045	.065	1.14	1.65	2, 8	
c1	.008	.015	.20	.38	8	
D	_	.405	_	10.29	4	
Е	.220	.310	5.59	7.87	4	
е	.100	BSC	2.54	BSC	5, 9	
eA	.300	BSC	7.62	BSC	7	
L	.125	.200	3.18	5.08		
Q	.015	.060	.38	1.52	3	
s1	.005	_	.13	_	6	
α	90°	105°	90°	105°		





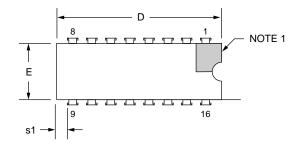
- Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
- 2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
- 3. Dimension "Q" shall be measured from the seating plane to the base plane.
- 4. This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
- 6. Applies to all four corners (leads number 1, 4, 5, and 8).
- 7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when " $\alpha$ " is  $90^\circ.$
- 8. All leads Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
- 9. Six spaces.

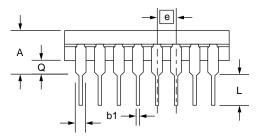


## **Mechanical Dimensions** (continued)

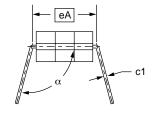
#### 16-Lead Ceramic DIP

Comple at	Inc	hes	Millimeters		Notes
Symbol	Min.	Max.	Min.	Max.	Notes
Α	_	.200	_	5.08	
b1	.014	.023	.36	.58	8
b2	.050	.065	1.27	1.65	2
c1	.008	.015	.20	.38	8
D	.745	.840	18.92	21.33	4
Е	.220	.310	5.59	7.87	4
е	.100	.100 BSC		BSC	5, 9
eA	.300	BSC	7.62	BSC	7
L	.115	.160	2.92	4.06	
Q	.015	.060	.38	1.52	3
s1	.005	_	.13	_	6
α	90°	105°	90°	105°	





- Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
- 2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 8, 9 and 16 only.
- 3. Dimension "Q" shall be measured from the seating plane to the base plane.
- 4. This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 16.
- 6. Applies to all four corners (leads number 1, 8, 9, and 16).
- "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "a" is 90°.
- 8. All leads Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
- 9. Fourteen spaces.



## **Ordering Information**

Part Number	Package	Operation Temperature Range
LM108D	8-Lead Ceramic DIP	-55°C to +125°C
LM108D/883B	8-Lead Ceramic DIP	-55°C to +125°C
LM108AD	8-Lead Ceramic DIP	-55°C to +125°C
LM108AD/883B	8-Lead Ceramic DIP	-55°C to +125°C
LM108T	8-Lead Metal Can TO-99	-55°C to +125°C
LM108T/883B	8-Lead Metal Can TO-99	-55°C to +125°C
LM108AT	8-Lead Metal Can TO-99	-55°C to +125°C
LM108AT/883B	8-Lead Metal Can TO-99	-55°C to +125°C
LH2108D	16-Lead Ceramic DIP	-55°C to +125°C
LH2108D/883B	16-Lead Ceramic DIP	-55°C to +125°C
LH2108AD	16-Lead Ceramic DIP	-55°C to +125°C
LH2108AD/883B	16-Lead Ceramic DIP	-55°C to +125°C

#### Note:

1. /883B suffix denotes Mil-Std-883, Level B processing

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com



# LM111/LH2111 Voltage Comparators

#### **Features**

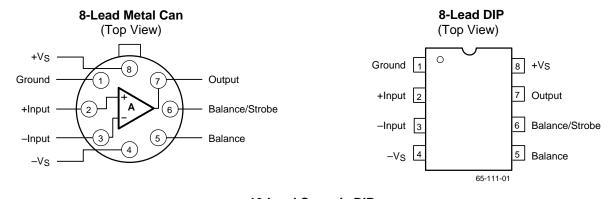
- Low input offset current 4 nA
- Low input bias current 60 nA
- Operates from a single +5V supply
- Response Time 200 ns

## **Description**

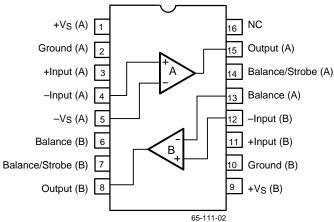
These low input current voltage comparators are designed to operate over a wide range of supply voltages, including +15V and single +5V supplies. Their outputs are compatible with DTL, RTL, TTL and MOS devices, and can be connected in "wire-OR" configuration. The LH2111 consists of two LM111 ICs packaged in a 16-lead DIP. The LH2111 is available with MIL-STD 883B screening.

LM11/LH2111 PRODUCT SPECIFICATION

## **Pin Assignments**



## 16-Lead Ceramic DIP (Top View)



## **Absolute Maximum Ratings**

Parameter	Min.	Max.	Unit
Supply Voltage	-18	+18	V
Output to -Vs		50	V
Ground to -Vs		30	V
Differential Input Voltage		30	V
Input Voltage <sup>1</sup>	-15	+15	V
Power Dissipation <sup>2</sup>		500	mW
Output Short Circuit Duration		10	seconds
Storage Temperature Range	-65	+150	°C
Operating Temperature Range	-55	+125	•C
Voltage at Strobe Pin		+Vs-5	V
Lead Soldering Temperature (60 seconds)		+300	°C

- 1. For supply voltages other than  $\pm 15$ V, the maximum input is equal to the supply voltage.
- 2. Observe package thermal characteristics.

PRODUCT SPECIFICATION LM111/LH2111

#### **Thermal Characteristics**

Parameter	8-Lead Metal Can	8-Lead Ceramic DIP	16-Lead Ceramic DIP
Maximum Junction Temperature	+175°C	+175°C	+175°C
Maximum PD TA <50°C	658 mW	833 mW	1042 mW
Thermal Resistance, θ <sub>JC</sub>	50°C/W	45°C/W	60°C/W
Thermal Resistance, θJA	190°C/W	150°C/W	120°C/W
For T <sub>A</sub> > 50°C Derate at	5.26 mW/°C	8.33 mW/°C	8.38 mW/°C

## **Electrical Characteristics**

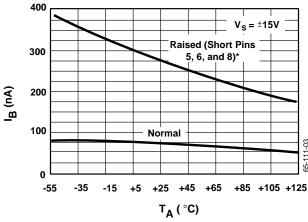
 $VS = \pm 15V^{1}$  and  $-55^{\circ}C \le TA \le +125^{\circ}C$  unless otherwise noted.

Parameters	Test Conditions	Min.	Тур.	Max.	Units
Input Offset Voltage <sup>2</sup>	$T_A = +25$ °C, Rs 50 kΩ		0.7	3.0	mV
Input Offset Current <sup>2</sup>	T <sub>A</sub> = +25°C		4.0	10	nA
Input Bias Current	TA = +25°C		60	100	nA
Large Signal Voltage Gain	T <sub>A</sub> = +25°C	40	200		V/mV
Response Time Output Voltage Low (V <sub>OL</sub> )	$T_A = +25$ °C, 100 mV step, 5 mV overdrive $V_{IN} \le 5$ mV, $I_L = 50$ mA, $T_A = +25$ °C		200 3.0		ns mA
Output Leakage current	VIN 25 mV, VOUT = 35V, T <sub>A</sub> = +25°C, ISTROBE = 3 mA		0.2	10	nA
Input Offset Voltage <sup>2</sup>	Rs ≤ 50 KΩ		1.5	4.0	mV
Input Offset Current <sup>2</sup>			5.0	20	nA
Input Bias Current			100	150	nA
Input Voltage Range	Pin 7 pull up may go to +5V	-14.5		13.0	V
Output Voltage Low (VOL)	$+VS = 4.5V$ , $-VS = 0V$ , $VIN \le -6$ mV, $IOUT = 8.0$ mA		0.23	0.4	V
Output Leakage Current	VIN ≥ 5 mV, VOUT = 35V		100	500	nA
Positive Supply Current	T <sub>A</sub> = +25°C, each amplifier		5.1	6.0	mA
Negative Supply Current	T <sub>A</sub> = +25°C, each amplifier		4.1	5.0	mA

- 1. Vos, los and lB specifications apply for  $Vs = \pm 15V$ .
- 2. Vos and los are maximum values required to drive the output to within 1V of either supply with a 1 mA load.
- 3. Do not short circuit the strobe pin to ground—drive it with a 3 to 5 mA current Instead.
- 4. If the strobe and balance pins are unused, short them together for maximum AC stability.

LM111/LH2111 PRODUCT SPECIFICATION

## **Typical Performance Characteristics**



<sup>\*</sup> Pin numbers are for 8-lead packages

Figure 1. Input Bias Current vs. Temperature

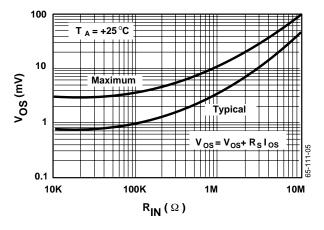


Figure 3. Equivalent Input Offset Voltage vs. Input Resistance

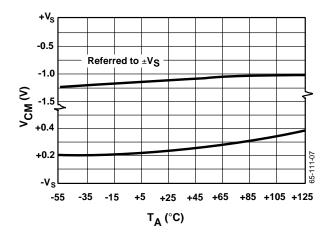
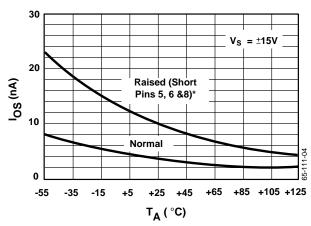


Figure 5. Common Mode Llmits vs. Temperature



<sup>\*</sup> Pin numbers are for 8-lead packages

Figure 2. Input Offset Current vs. Temperature

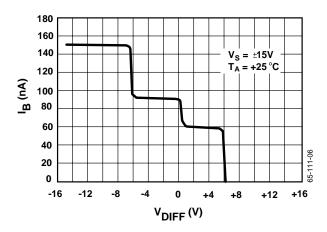


Figure 4. Input Bias Current vs. Differential Input Voltage

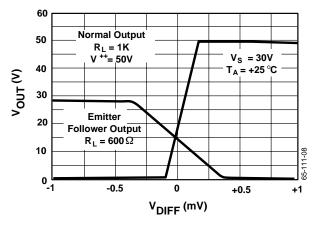


Figure 6. Output Voltage vs. Differential Input Voltage

PRODUCT SPECIFICATION LM111/LH2111

## **Typical Performance Characteristics** (continued)

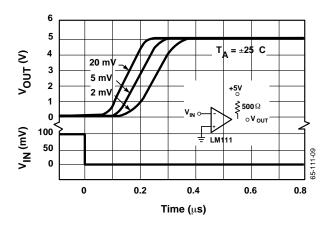


Figure 7. Input Overdrive vs. Response Times

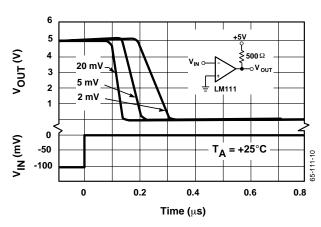


Figure 8. Input Overdrive vs. Response Times

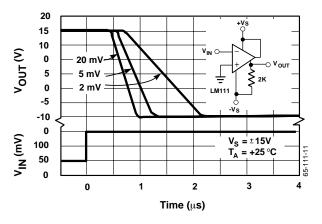


Figure 9. Input Overdrive vs. Response Times

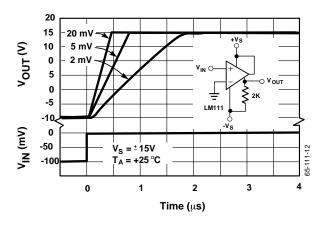


Figure 10. Input Overdrive vs. Response Times

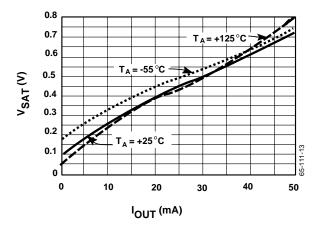


Figure 11. OpenSaturation Voltage vs. Output Current

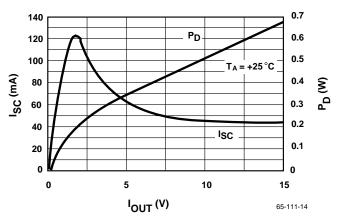
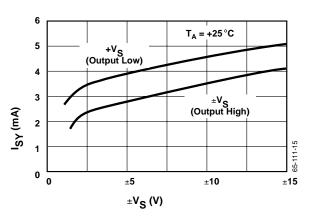


Figure 12. Short Circuit Current, Power Dissipation vs. Output Voltage

LM11/LH2111 PRODUCT SPECIFICATION

## **Typical Performance Characteristics** (continued)



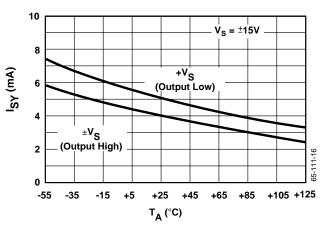


Figure 13. Supply Current vs. Supply Voltage

Figure 14. Supply Current vs. Temperature

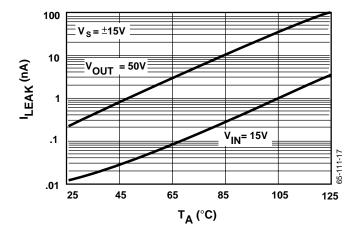


Figure 15. Leakage Current vs. Temperature

PRODUCT SPECIFICATION LM111/LH2111

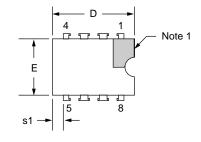
LM111/LH2111 PRODUCT SPECIFICATION

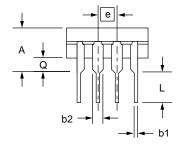
PRODUCT SPECIFICATION LM111/LH2111

## **Mechanical Dimensions**

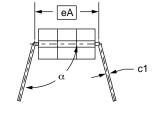
#### **8-Lead Ceramic DIP**

Symbol	Inches		Millin	neters	Notes
Syllibol	Min.	Max.	Min.	Max.	Notes
Α	_	.200	_	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2, 8
c1	.008	.015	.20	.38	8
D	1	.405		10.29	4
E	.220	.310	5.59	7.87	4
е	.100	BSC	2.54 BSC		5, 9
eA	.300	BSC	7.62	BSC	7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	_	.13	_	6
α	90°	105°	90°	105°	





- Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
- 2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 4, 5 and 8 only.
- 3. Dimension "Q" shall be measured from the seating plane to the base plane.
- 4. This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 8.
- 6. Applies to all four corners (leads number 1, 4, 5, and 8).
- 7. "eA" shall be measured at the center of the lead bends or at the centerline of the leads when " $\alpha$ " is 90°.
- 8. All leads Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
- 9. Six spaces.

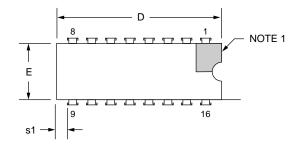


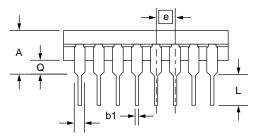
LM11/LH2111 PRODUCT SPECIFICATION

# **Mechanical Dimensions** (continued)

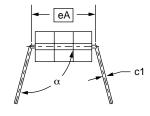
#### 16-Lead Ceramic DIP

Comple at	Inches		Millim	Millimeters		
Symbol	Min.	Max.	Min.	Max.	Notes	
Α	_	.200	_	5.08		
b1	.014	.023	.36	.58	8	
b2	.050	.065	1.27	1.65	2	
c1	.008	.015	.20	.38	8	
D	.745	.840	18.92	21.33	4	
Е	.220	.310	5.59	7.87	4	
е	.100	BSC	2.54	BSC	5, 9	
eA	.300	BSC	7.62	BSC	7	
L	.115	.160	2.92	4.06		
Q	.015	.060	.38	1.52	3	
s1	.005	_	.13	_	6	
α	90°	105°	90°	105°		





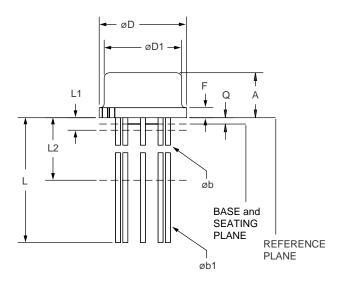
- Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
- 2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 8, 9 and 16 only.
- 3. Dimension "Q" shall be measured from the seating plane to the base plane.
- 4. This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 16.
- 6. Applies to all four corners (leads number 1, 8, 9, and 16).
- "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "a" is 90°.
- All leads Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
- 9. Fourteen spaces.

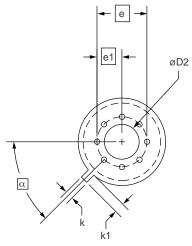


PRODUCT SPECIFICATION LM111/LH2111

# **Mechanical Dimensions** (continued)

## 8-Lead Metal Can (TO-99)





Cumb al	Inc	hes	Millin	neters	Netes
Symbol	Min.	Max.	Min.	Max.	Notes
А	.165	.185	4.19	4.70	
øb	.016	.019	.41	.48	1, 5
øb1	.016	.021	.41	.53	1, 5
øD	.335	.375	8.51	9.52	
øD1	.305	.335	7.75	8.51	
øD2	.110	.160	2.79	4.06	
е	.200	BSC	5.08 BSC		
e1	.100	BSC	2.54 BSC		
F	_	.040	_	1.02	
k	.027	.034	.69	.86	
k1	.027	.045	.69	1.14	2
L	.500	.750	12.70	19.05	1
L1	_	.050	_	1.27	1
L2	.250	_	6.35	_	1
Q	.010	.045	.25	1.14	
α	45°	BSC	45°	BSC	

- (All leads) øb applies between L1 & L2. øb1 applies between L2 & .500 (12.70mm) from the reference plane. Diameter is uncontrolled in L1 & beyond .500 (12.70mm) from the reference plane.
- 2. Measured from the maximum diameter of the product.
- 3. Leads having a maximum diameter .019 (.48mm) measured in gauging plane, .054 (1.37mm) +.001 (.03mm) -.000 (.00mm) below the reference plane of the product shall be within .007 (.18mm) of their true position relative to a maximum width tab.
- 4. The product may be measured by direct methods or by gauge.
- All leads increase maximum limit by .003 (.08mm) when lead finish is applied.

PRODUCT SPECIFICATION LM111/LH2111

# **Ordering Information**

Part Number	Package	Operating Temperature Range
LM111T/883B	8-Lead Metal Can (TO-99)	-55°C to +125°C
LM111D/883B	8-Lead Ceramic DIP	-55°C to +125°C
LH2111D	16-Lead Ceramic DIP	-55°C to +125°C
LH2111D/883B	16-Lead Ceramic DIP	-55°C to +125°C

#### Note:

1. /883 B suflix denotes MIL-STD-883, Level B processing

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com



# LM124/LM324 Single-Supply Quad Operational Amplifier

#### **Features**

- Large DC voltage gain—100 dB
- · Compatible with all forms of logic
- · Temperature compensated
- Unity Gain Bandwidth—1 MHz
- Large output voltage swing—0V to (+VS -1.5V)
- · Input common mode voltage range includes ground

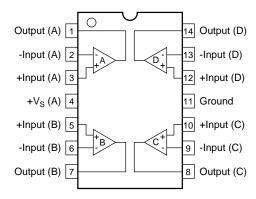
# **Description**

Each of the devices in this series consists of four independent high-gain operational amplifiers that are designed for single-supply operation. Operation from split power supplies is also possible and the low power supply drain is independent of the magnitude of the power supply voltage.

Used with a dual supply, the circuit will operate over a wide range of supply voltages. However, a large amount of cross-over distortion may occur with loads to ground. An external current-sinking resistor to -Vs will reduce crossover distortion. There is no crossover distortion problem in single-supply operation if the load is direct-coupled to ground.

LM124/LM324 PRODUCT SPECIFICATION

# **Pin Assignments**



# **Absolute Maximum Ratings**

Parameter	Conditions	Min.	Max.	Units
Supply Voltage			+32 or ±16	V
Differential Input Voltage			32	V
Input Voltage		-0.3	+32	V
Output Short Circuit to Ground <sup>1</sup>	One Amplifier +V <sub>S</sub> ≤ 15V and T <sub>A</sub> = +25°C	Continuous		
Input Current <sup>2</sup>	VIN < -0.3V		50	mA
Operating Temperature Range				
LM124		-55	+125	°C
LM324		0	+70	°C

#### Notes:

- Short circuits from the output to +Vs can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of +Vs. At values of supply voltage in excess d +Vs, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.
- 2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the +Vs voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage again returns to a value greater than 0.3V.

#### **Thermal Characteristics**

Parameter	SOIC	Plastic DIP	Ceramic DIP
Maximum Junction Temperature	+125°C	+125°C	+175°C
Max. PD TA < 50°C	300 mW	468 mW	1042 mW
Thermal Resistance, θJC	_	_	60°C/W
Thermal Resistance, θJA	200°C/W	160°C/W	120°C/W
For T <sub>A</sub> > 50°C Derate at	5.0 mW/°C	6.25 mW/°C	8.38 mW/°C

PRODUCT SPECIFICATION LM124/LM324

#### **Electrical Characteristics**

 $+V_S = +5.0V$  (see Note 1) and  $T_A = +25^{\circ}C$ , unless otherwise noted.

				LM124			LM324		
Paramet	ers	Test Conditions	Min.	Тур.	Max.	Min.	Тур.	Max.	Units
Input Offset Vo	ltage <sup>1</sup>			±2.0	±5.0		±2.0	±7.0	mV
Input Bias Curi	ent <sup>2</sup>			45	150		45	250	nA
Input Offset Cu	irrent			±3.0	±30		±5.0	±50	nA
Input Voltage F	Range <sup>3</sup>	+VS = +30V	0		+Vs-1.5	0		+Vs-1.5	V
Supply Current		R <sub>L</sub> = ∞, +V <sub>S</sub> = 30V		1.5	3.0		1.5	3.0	mA
(Over Tempera	iture)	R <sub>L</sub> = ∞ on all op amps		0.7	1.2		0.7	1.2	mA
Large Signal V Gain	oltage	+V <sub>S</sub> = 15V (for large V <sub>OUT</sub> swing) $R_L \ge 2 K\Omega$	50	100		25	100		V/mV
Output	Vон	+Vs = +30V, $R_L = 2K\Omega$	26			26			V
Voltage Swing	Vон	R <sub>L</sub> ≥ 10 KΩ	27	28		27	28		V
	VoL	+Vs = +5.0V, RL = 10KΩ		5.0	20		5.0	20	mV
Common Mode Rejection Ratio			70	85		65	70		dB
Power Supply Rejection Ratio	)		65	100		65	100		dB
Channel Separ	ation <sup>4</sup>	F = 1 KHz to 20 KHz (Input referred)		-120			-120		dB
Output Current	Source	VIN+ = 1V, VIN- = 0V, +VS = 15V	20	40		20	40		mA
	Sink	VIN- = 1V, VIN+ = 0V, +VS = 15V	10	20		10	20		mA
		V <sub>IN+</sub> = 1V, V <sub>IN-</sub> = 0V, +V <sub>OUT</sub> = 200 mV	12	50		12	50		μΑ

- 1. VOUT = 1.4V,  $RS = 0\Omega$  with +VS from 5V to 30V; and over the full common mode range (0V to +VS-1.5V).
- 2. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
- 3. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is +Vs-1.5V, but either or both inputs can go to +32V without damage.
- 4. Due to proximity of external components, ensure that coupling is not originating via stray capacitance between these externall parts. This typically can be detected as this type of capacitance increases at higher frequencies.

LM124/LM324 PRODUCT SPECIFICATION

#### **Electrical Characteristics**

 $+V_S = +5.0V$ , LM124 =  $-55^{\circ} \le T_A \le 125^{\circ}C$ , LM324 =  $0^{\circ}C \le T_A \le 70^{\circ}C$  unless other wise noted.

				LM124			LM324		
Parameters		Conditions	Min.	Тур.	Max .	Min.	Тур.	Max.	Unit
Short Circuit Curren	t <sup>1</sup>	T <sub>A</sub> = +25°C		40	60		40	60	mA
Input Offset Voltage	2				±7.0			±9.0	mV
Input Offset Voltage	Drift	$R_S = 0\Omega$		7.0			7.0		μV/°C
Input Offset Current					±100			±150	nA
Input Offset Current	Drift			10			10		pA/°C
Input Bias Current <sup>3</sup>				40	300		40	500	nA
Input Voltage Range	$e^4$	+Vs = +30V	0		+Vs-2.0	0		+Vs-2.0	V
Large Signal Voltage Gain		+Vs - +15V (For Large V <sub>OUT</sub> Swing) R <sub>L</sub> $\geq$ 2.0 KΩ	25			15			V/mV
Output Voltage Swing	Voн	+VS = +30V, RL = 2 KΩ	26			26			V
	Voн	R <sub>L</sub> ≥ 10 KΩ	27	28		27	28		V
	VoL	$+V_S = +5.0V,$ R <sub>L</sub> = 10 KΩ		5.0	20		5.0	20	mV
Output Current	Source	VIN+ = +1.0V, VIN- = 0V, +VS = +15V	10	20		10	20		mA
Sink		V <sub>IN</sub> -= +1.0V, V <sub>IN</sub> += 0V, +VS = +15V	5.0	8.0		5.0	8.0		mA
Differential Input Vo	Itage <sup>4</sup>				+Vs			+Vs	V

- Short circuits from the output to +Vs can cause excessive heating and eventual destruction. The maximum output current is approximately 40 mA independent of the magnitude of +Vs. At values of supply voltage in excess of +Vs, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on an amplifiers.
- 2. VOUT =1.4V, Rs =  $0\Omega$  with +Vs from 5V to 30V and over the full common mode range (0V to +Vs -1.5V).
- 3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
- 4. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is +Vs -1.5V, but either or both inputs can go to +32V without damage.

PRODUCT SPECIFICATION LM124/LM324

# **Typical Performance Characteristics**

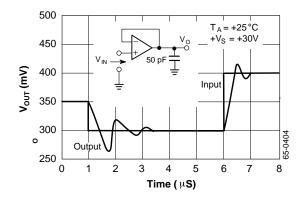


Figure 1. Follower Small Signal Pulse Response

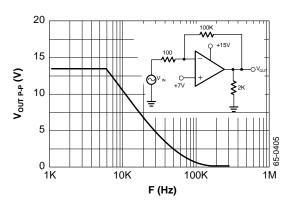


Figure 2. Output Voltage Swing vs. Frequency

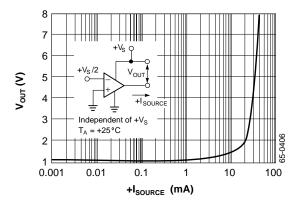


Figure 3. Output Voltage vs. Output Source Current

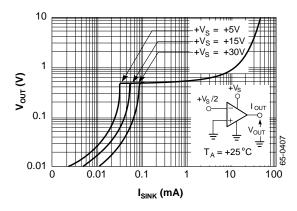


Figure 4. Output Voltage vs. Output Sink Current

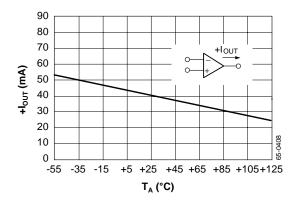


Figure 5. Current Limiting Output Current vs. Temperature

LM124/LM324 PRODUCT SPECIFICATION

# **Typical Performance Characteristics** (continued)

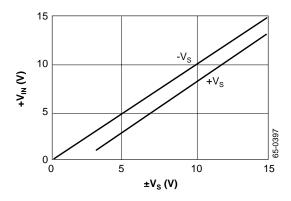


Figure 6. Input Voltage vs. Supply Voltage

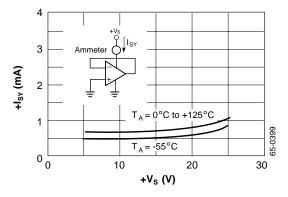


Figure 8. Supply Current vs. Supply Voltage

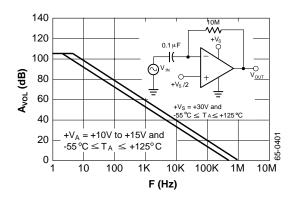


Figure 10. Open Loop Voltage Gain vs. Frequency

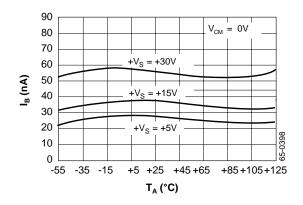


Figure 7. Input Bias Current vs. Temperature

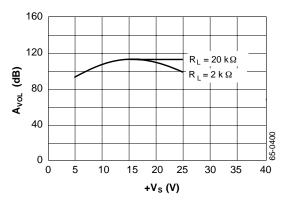


Figure 9. Open Loop Voltage Gain vs. Supply Voltage

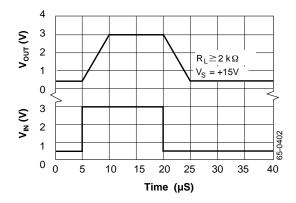


Figure 11. Follower Large Pulse Response Signal vs. Time

PRODUCT SPECIFICATION LM124/LM324

LM124/LM324 PRODUCT SPECIFICATION

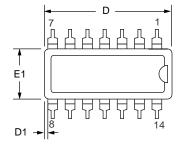
PRODUCT SPECIFICATION LM124/LM324

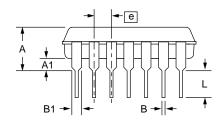
# **Mechanical Dimensions**

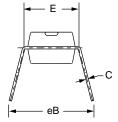
#### 14-Lead Plastic DIP

Cumbal	Inches		Millim	neters	Notes
Symbol	Min.	Max.	Min.	Max.	Notes
Α	_	.210	_	5.33	
A1	.015	_	.38	_	
A2	.115	.195	2.93	4.95	
В	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
С	.008	.015	.20	.38	4
D	.725	.795	18.42	20.19	2
D1	.005	_	.13	_	
E	.300	.325	7.62	8.26	
_E1	.240	.280	6.10	7.11	2
е	.100	BSC	2.54 BSC		
eB	_	.430	_	10.92	
L	.115	.200	2.92	5.08	
N	1	4	1	4	5

- 1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- 2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
- 3. Terminal numbers are shown for reference only.
- 4. "C" dimension does not include solder finish thickness.
- 5. Symbol "N" is the maximum number of terminals.





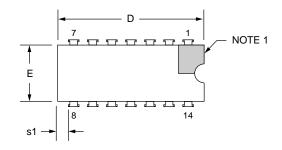


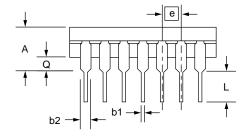
LM124/LM324 PRODUCT SPECIFICATION

# **Mechanical Dimensions** (continued)

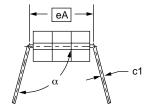
#### 14-Lead Ceramic DIP

Comple at	Inches		Millim	neters	Notes
Symbol	Min.	Max.	Min.	Max.	Notes
Α	_	.200	_	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	8
D		.785		19.94	4
Е	.220	.310	5.59	7.87	4
е	.100	BSC	2.54	BSC	5, 9
eA	.300	BSC	7.62	BSC	7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	_	.13	_	6
α	90°	105°	90°	105°	





- Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
- 2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 7, 8 and 14 only.
- 3. Dimension "Q" shall be measured from the seating plane to the base plane.
- 4. This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 14.
- 6. Applies to all four corners (leads number 1, 7, 8, and 14).
- "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "a" is 90°.
- All leads Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
- 9. Twelve spaces.



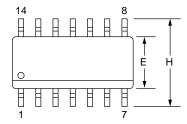
PRODUCT SPECIFICATION LM124/LM324

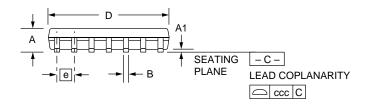
# **Mechanical Dimensions** (continued)

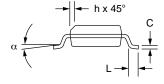
#### 14-Lead SOIC

Cumbal	Inches		Millin	neters	Notes
Symbol	Min.	Max.	Min.	Max.	Notes
Α	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
В	.013	.020	0.33	0.51	
С	.008	.010	0.19	0.25	5
D	.336	.345	8.54	8.76	2
Е	.150	.158	3.81	4.01	2
е	.050	BSC	1.27 BSC		
Н	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	1	4	14		6
α	0°	8°	0°	8°	
ccc	_	.004	_	0.10	

- 1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- 2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
- 3. "L" is the length of terminal for soldering to a substrate.
- 4. Terminal numbers are shown for reference only.
- 5. "C" dimension does not include solder finish thickness.
- 6. Symbol "N" is the maximum number of terminals.







PRODUCT SPECIFICATION LM124/LM324

# **Ordering Information**

Part Number	Package	Operating Temperature Range
LM324M	14-Lead Plastic SOIC	0°C to +70°C
LM324N	14-Lead Plastic DIP	0°C to +70°C
LM124D	14-Lead Ceramic DIP	-55°C to +125°C
LM124D/883B	14-Lead Ceramic DIP	-55°C to +125°C

#### Note:

1. 883B suffix denotes Mil-Std-883, Level B processing.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com



# LM139/LM139A, LM339 Single Supply Quad Comparators

#### **Features**

- · Input common mode voltage range includes ground
- Wide single supply voltage range—2V to 36V
- Output compatible with TTL, DTL, ECL, MOS and CMOS logic systems
- Very low supply current drain (0.8 mA) independent of supply voltage

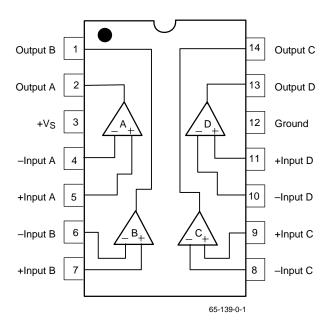
# **Description**

These devices offer higher frequency operation and faster switching than can be had from internally compensated quad op amps. Intended for single supply applications, the Darlington PNP input stage allows them to compare voltages that include ground. The two stage common-emitter output circuit provides gain and output sink capacity of 3.2 mA at an output level of 400 mV. The output collector is left open, permitting the designer to drive devices in the range of 2V to 36V.

They are intended for applications not needing response time less than 1  $\mu$ s, but demanding excellent op amp input parameters to offset voltage, current and bias current, to ensure accurate comparison with a reference voltage.

LM139/LM139A, LM339 PRODUCT SPECIFICATION

# **Pin Assignments**



# **Absolute Maximum Ratings**

Parameter	Min.	Max.	Unit.
Supply Voltage	-8	+36 or +8	V
Differential Input Voltage		36	V
Input Voltage Range <sup>2</sup>	-0.3	+36	V
Output Short Circuit to Ground <sup>1</sup>		Continuous	
Input Current (VIN < -0.3V) <sup>(2)</sup>		50	mA
Operating Temperature Range			
LM139	-55	+125	°C
LM339	0	+70	°C
Storage Temperature Range	-65	150	°C
Lead Soldering Temperature			
SOIC, 10 seconds		+260	°C
DIP, 60 seconds		+300	°C

- 1. Short circuits from the output to +Vs can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of +Vs.
- 2. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltage of the comparators to go to the +Vs voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and nominal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3V.

PRODUCT SPECIFICATION LM139/LM139A, LM339

#### Thermal Characteristics

Parameter	SOIC	Plastic DIP	Ceramic DIP
Maximum Junction Temperature	+125°C	+125°C	+175°C
Maximum PD TA <50°C	300 mW	468 mW	1042mW
Thermal Resistance, θ <sub>JC</sub>	_	_	60°C/W
Thermal Resistance, θJA	200°C/W	160°C/W	120°C/W
For T <sub>A</sub> > 50°C Derate at	5.0 mW/°C	6.25 mW/°C	8.33 mW/°C

#### **Electrical Characteristics**

 $V_S = +5V$ , see Note 1.

		LM139A			
Parameters	Test Conditions	Min.	Тур.	Max.	Unit
Input Offset Voltage	$T_A = +25^{\circ}C^2$		±1.0	±2.0	mV
Input Bias Current	Output In Linear Range T <sub>A</sub> = +25°C <sup>3</sup> , V <sub>CM</sub> = 0V		25	100	nA
Input Offset Current	TA = +25°C, $VCM = 0V$		±3.0	±25	nA
Input Voltage Range	$T_A = +25^{\circ}C^4$ , $V_S = 30V$			+Vs-1.5	V
Supply Current	R <sub>L</sub> = ∞ on all comparators, T <sub>A</sub> = +25°C		0.8	2.5	mA
Large Signal Voltage Gain	R <sub>L</sub> = $\infty$ , +V <sub>S</sub> = 30V, R <sub>L</sub> $\ge$ 15 KΩ, +V <sub>S</sub> = +5V (to support large V <sub>OUT</sub> swing) T <sub>A</sub> = +25°C	50	200		V/mV
Large Signal Response Time	$V_{IN}$ = TTL Logic Swing, $V_{REF}$ = 1.4V, $V_{RL}$ = 5V, $R_L$ = 5.1 $K\Omega$ , $T_A$ = +25°C		300		ns
Response Time	$V_{RL} = 5V$ , $R_{L} = 5.1$ $K_{Ω}$ , $T_{A} = +25^{\circ}C^{5}$		1.3		μS
Output Sink Current	$V_{IN-} \ge 1V$ , $V_{IN+} = 0$ , $V_{OUT} \le 1.5V$ , $T_A = +25^{\circ}C$	6.0	16		mA
Saturation Voltage	VIN- ≥ 1V, VIN+ = 0, ISINK ≤ 4 mA, TA = 25°C		250	400	mV
Output Leakage Current	V <sub>IN+</sub> ≥ 1V, V <sub>IN-</sub> = 0, V <sub>OUT</sub> = 5V, T <sub>A</sub> = +25°C		0.1		μΑ
Input Offset Voltage <sup>2</sup>				±4.0	mV
Input Offset Current	V <sub>CM</sub> = 0V			±100	nA
Input Bias Current	VCM = 0V			300	nA
Input Voltage Range	+VS = 30V	0		+Vs-2.0	V
Saturation Voltage	V <sub>IN-</sub> ≥ 1V, V <sub>IN+</sub> = 0, I <sub>SINK</sub> ≤ 4 mA			700	mV
Output Leakage Current	VIN+ ≥ 1V, VIN- = 0, VOUT = 30V			1.0	μΑ
Differential Input Voltage <sup>7</sup>	$V_{IN+} \ge 0V$ , (or -Vs, if used) <sup>6</sup>			36	V

- 1. These specifications apply for +Vs = 5V and -55°C  $\leq$  TA  $\leq$  +125°C, unless otherwise stated. The LM339 temperature specifications are limped to 0°C  $\leq$  TA  $\leq$  +70°C.
- 2. At output switch points VOUT = 1.4V, RS =  $0\Omega$  with +VS from 5V to 30V; and over the full input common mode range (VOUT to +VS-1.5V).
- 3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
- 4. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is +Vs-1.5V, but either or both inputs can go to +30V without damage.
- 5. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained. See Typical Performance Characteristics section.
- 6. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common mode range, the comparator will provide a proper output state. The low input voltage stage must not be less than -0.3V (or 0.3V below the magnitude of the negative power supply, if used).
- 7. Guaranteed by design.

LM139/LM139A, LM339 PRODUCT SPECIFICATION

#### **Electrical Characteristics**

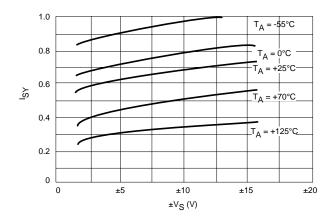
Vs = +5V, see Note 1.

			LM139			LM339		
Parameters	Test Conditions	Min	Тур	Max	MIn	Тур	Max	Units
Input Offset Voltage	$T_A = +25^{\circ}C^2$		±2.0	±5.0		±2.0	±5.0	mV
Input Bias Current	Output in Linear Range $T_A = +25^{\circ}C^3$ , $V_{CM} = 0V$		25	100		25	250	nA
Input Offset Current	$T_A = +25^{\circ}C$ , $V_{CM} = 0V$		±3.0	±25		±5.0	±50	nA
Input Voltage Range	$T_A = +25^{\circ}C^4$ , +VS = 30V	0		+Vs -1.5	0		+VS -1.5	V
Supply Cunent	R <sub>L</sub> = ∞ on all comparators, T <sub>A</sub> = +25°C		0.8	2.5		0.8	2.5	mA
Large Signal Voltage Gain	$R_L = \infty + V_S = 30V$ , $R_L \ge 15 \text{ K}\Omega$ , $+V_S = +5V$ (to support large VOUT swing), $T_A = +25^{\circ}C$	25	200			200		V/mV
Large Signal Response Time	$V_{IN}$ = TTL Logic Swing, $V_{REF}$ = 1.4V, $V_{RL}$ = 5V, $R_L$ = 5.1 K $\Omega$ , $T_A$ = +25°C		300			300		ns
Response Time	$V_{RL} = 5V$ , $R_{L} = 5.1$ $K_{Ω}$ $T_{A} = +25^{\circ}C^{5}$		1.3			1.3		μS
Output Sink Current	VIN- ≥ 1V, VIN+ = 0, VOUT ≤ 1.5V, TA = +25°C	6.0	16		6.0	16		mA
Output Voltage, VOL	$V_{IN} \ge 1V$ , $V_{IN+} = 0$ , $I_{SINK} \le 4$ mA, $T_A = +25$ °C		250	400		250	400	mV
Output Leakage Current	$V_{IN+} \ge 1V$ , $V_{IN-} = 0$ , $V_{OUT} = 5V$ , $T_A = +25$ °C		0.1			0.1		μΑ
Input Offset Voltage <sup>2</sup>				±9.0			±9.0	mV
Input Offset Current				±100			±150	nA
Input Bias Current	VCM = 0V			300			400	nA
Input Voltage Range	VcM = 30V	0		+Vs -2.0	0		+Vs -2.0	V
Output Voltage VOL	VIN- ≥ 1V, VIN+ = 0 ISINK ≤ 4 mA			700			700	mV
Output Leakage Cunent	VIN+ ≥ 1V, VIN- = 0 VOUT = 30V			1.0			1.0	μΑ
Differential Input Voltage <sup>7</sup>	$V_{IN+} \ge 0V \text{ (or -Vs, if used)}^6$			36			36	V

- 1. These specifications apply for +Vs = 5V and -55°C ≤ TA ≤ +125°C, unless otherwise stated. The LM339 temperature specifications are limped to 0°C ≤ TA ≤ +70°C.
- 2. At output switch points  $V_{OUT} = 1.4V$ ,  $R_S = 0\Omega$  with +Vs from 5V to 30V; and over the full input common mode range ( $V_{OUT}$  to +Vs-1.5V).
- 3. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
- 4. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common mode voltage range is +Vs-1.5V, but either or both inputs can go to +30V without damage.
- 5. The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained. See Typical Performance Characteristics section.
- 6. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common mode range, the comparator will provide a proper output state. The low input voltage stage must not be less than -0.3V (or 0.3V below the magnitude of the negative power supply, if used).
- 7. Guaranteed by design.

PRODUCT SPECIFICATION LM139/LM139A, LM339

# **Typical Performance Characteristics**



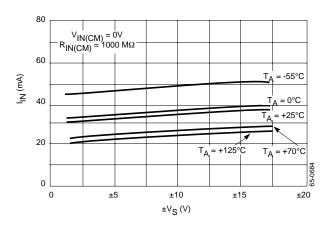


Figure 1. Supply Current vs. Supply Voltage

Figure 2. Input Current vs. Supply Voltage

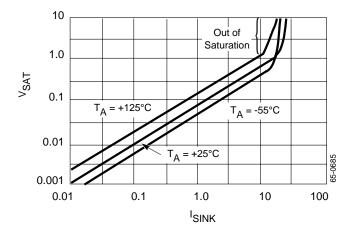


Figure 3. Output Saturation Voltage vs. Sink Current

LM139/LM139A, LM339 PRODUCT SPECIFICATION

# **Typical Performance Characteristics** (continued)

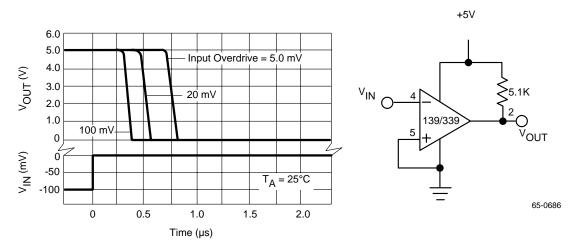


Figure 4. Input Overdriver Repsonse Time

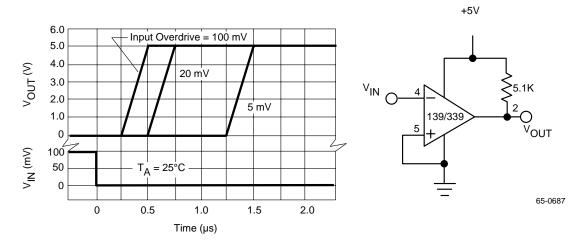


Figure 5. Input Overdrive Response Time

PRODUCT SPECIFICATION LM139/LM139A, LM339

# **Applications**

Single Supply (+Vs = +15V).

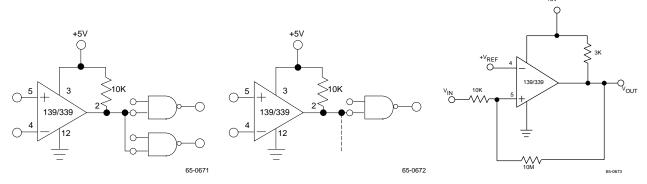


Figure 6. Driving TTL

Figure 7. Driving CMOS

Figure 8. Comparator with Hysteresis

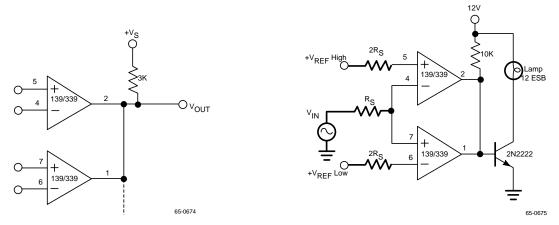


Figure 9. ORing the Output

Figure 10. Limit Comparator

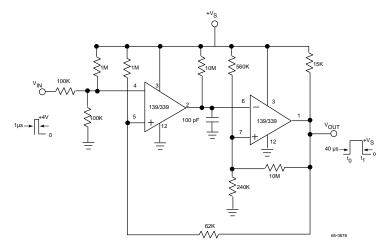


Figure 11. One-Shot Multivibrator with Input Lock Out

LM139/LM139A, LM339 PRODUCT SPECIFICATION

# **Applications** (continued)

Single Supply (+Vs = +15V).

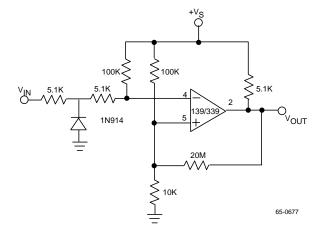


Figure 12. Zero Crossing Detector (Single Power Supply)

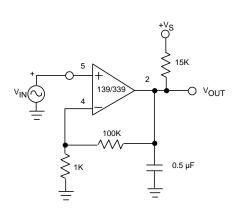


Figure 13. Low Frequency Op Amp

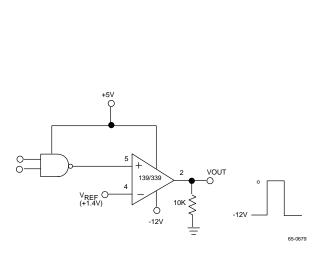


Figure 14. TTL to MOS Logic Converter

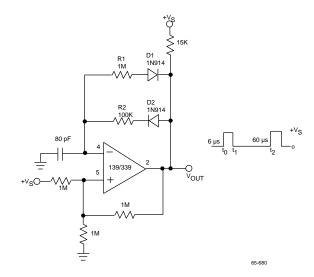


Figure 15. Pulse Generator

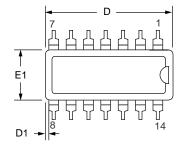
PRODUCT SPECIFICATION LM139/LM139A, LM339

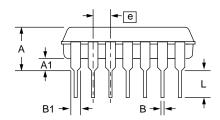
# **Mechcanical Dimensions**

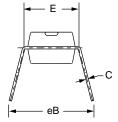
#### 14-Lead Plastic DIP

Cumbal	Inc	Inches		Millimeters		
Symbol	Min.	Min. Max. M		Max.	Notes	
Α	_	.210	_	5.33		
A1	.015	_	.38	_		
A2	.115	.195	2.93	4.95		
В	.014	.022	.36	.56		
B1	.045	.070	1.14	1.78		
С	.008	.015	.20	.38	4	
D	.725	.795	18.42	20.19	2	
D1	.005	_	.13	_		
E	.300	.325	7.62	8.26		
_E1	.240	.280	6.10	7.11	2	
е	.100	BSC	2.54	BSC		
eВ	_	.430	_	10.92		
L	.115	.200	2.92	5.08		
N	14		1	5		

- 1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- 2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
- 3. Terminal numbers are shown for reference only.
- 4. "C" dimension does not include solder finish thickness.
- 5. Symbol "N" is the maximum number of terminals.







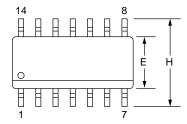
LM139/LM139A, LM339 PRODUCT SPECIFICATION

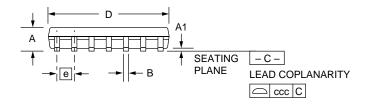
# **Mechanical Dimensions** (continued)

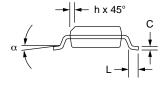
#### 14-Lead Plastic SOIC

Cumbal	Inc	hes	Millin	Notes	
Symbol	Min.	Max.	Min.	Max.	Notes
Α	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
В	.013	.020	0.33	0.51	
С	.008	.010	0.19	0.25	5
D	.336	.345	8.54	8.76	2
Е	.150	.158	3.81	4.01	2
е	.050	.050 BSC		BSC	
Н	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	1	4	14		6
α	0°	8°	0°	8°	
ccc	_	.004	_	0.10	

- 1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- 2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
- 3. "L" is the length of terminal for soldering to a substrate.
- 4. Terminal numbers are shown for reference only.
- 5. "C" dimension does not include solder finish thickness.
- 6. Symbol "N" is the maximum number of terminals.





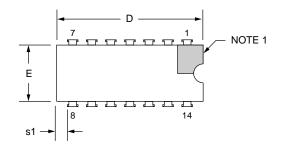


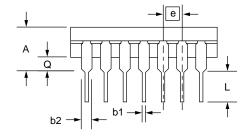
PRODUCT SPECIFICATION LM139/LM139A, LM339

# **Mechanical Dimensions** (continued)

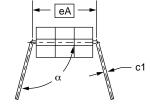
#### 14-Lead Ceramic DIP

Cumbal	Inc	hes	Millin	neters	Notes
Symbol	Min.	Max.	Min.	Max.	Notes
Α	_	.200	_	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	8
D		.785		19.94	4
Е	.220	.310	5.59	7.87	4
е	.100	.100 BSC		BSC	5, 9
eA	.300	BSC	7.62	BSC	7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	_	.13	_	6
α	90°	105°	90°	105°	





- Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
- 2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 7, 8 and 14 only.
- 3. Dimension "Q" shall be measured from the seating plane to the base plane.
- 4. This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 14.
- 6. Applies to all four corners (leads number 1, 7, 8, and 14).
- "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "a" is 90°.
- 8. All leads Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
- 9. Twelve spaces.



PRODUCT SPECIFICATION LM139/LM139A, LM339

# **Ordering Information**

Part Number	Package	Operating Temperature Range
LM339M	14-Lead Plastic SOIC	0°C to +70°C
LM339N	14-Lead Plastic DIP	0°C to +70°C
LM139D	14-Lead Ceramic DIP	-55°C to +125°C
LM139D/883B	14-Lead Ceramic DIP	-55°C to +125°C
LM139AD	14-Lead Ceramic DIP	-55°C to +125°C
LM139AD/883B	14-Lead Ceramic DIP	-55°C to +125°C

#### Notes:

1. /883B suffix denotes MIL-STD-883, Level B processing

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

#### **DUAL OPERATIONAL AMPLIFIERS**

The LM1458 series are dual general purpose operational amplifiers, having short circuits protected and require no external components for frequency compensation.

High common mode voltage range and absence of "latch up" make the LM1458 ideal for use as voltage followers.

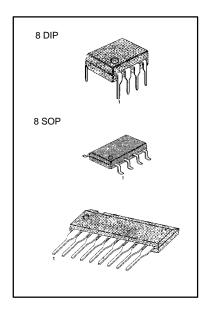
The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier and general feedback applications.

#### **FEATURES**

- Internal frequency compensation
- Short circuit protection

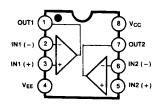
9 SIP

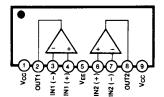
- Large common mode and differential voltage range
- No latch up
- Low power consumption



#### **BLOCK DIAGRAM**

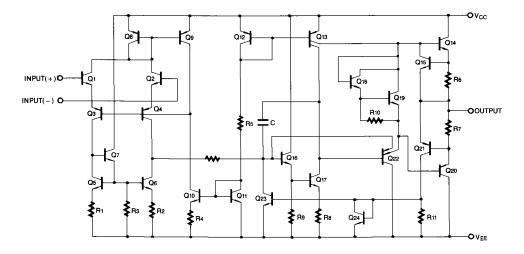
#### **ORDERING INFORMATION**





Device	Package	Operating Temperature
LM1458N	8 DIP	
LM1458AN	0	
LM1458S	9 SIP	0 ~ + 70°C
LM1458AS	5	0-4700
LM1458M	8 SOP	
LM1458AM	0	
LM1458IN	8 DIP	
LM1458AIN	0 Dii	
LM1458IS	9 SIP	-25 ~ + 85°C
LM1458AIS	5 51	23 + 03 0
LM1458IM	8 SOP	
LM1458AIM	0 001	

#### **SCHEMATIC DIAGRAM**



#### **ABSOLUTE MAXIMUM RATINGS**

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V <sub>cc</sub>	±18	V
Input Differential Voltage	$V_{I(DIFF)}$	30	V
Input Voltage	$V_{I}$	±15	V
Operating Temperature Range LM1458I/AI	$T_{OPR}$	- 25 ~ + 85	°C
LM1458/A		0 ~ + 70	°C
Storage Temperature Range	$T_{STG}$	- 65 ~ <b>+</b> 150	°C



#### **ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub> = + 15V, V<sub>EE</sub> = - 15V,  $T_A$  = 25 °C unless otherwise specified)

Characteristic	Cumbal	Test Conditions	LM	1458 <i>A</i>	/AI	L	M145	8/I	I Imia
Characteristic	Symbol	rest Conditions		Тур	Max	Min	Тур	Max	Unit
Input Offset Voltage	V <sub>IO</sub>	R <sub>S</sub> ≤10KΩ		2.0	6.0		2.0	10	mV
Input Offset Current	I <sub>IO</sub>			20	200		20	300	nA
Input Bias Current	I <sub>BIAS</sub>			80	500		80	700	nA
Large Signal Voltage Gain	$G_V$	$V_{O(P-P)} = \pm 10V, R_L \ge 2.0K\Omega$	20	200		20	200		V/mV
Input Voltage Range	$V_{I(R)}$		± 12	± 13		± 11	± 13		V
Input Resistance	Rı		0.3	1.0		0.3	1.0		ΜΩ
Common Mode Rejection Ratio	CMRR		70	90		60	90		dB
Power Supply Rejection Ratio	PSRR		77	90		77	90		dB
Supply Current (Both Amplifier)	Icc			2.3			2.3	8.0	mA
Output Voltage Swing	$V_{O(P.P)}$	R <sub>S</sub> ≤10KΩ	± 12	± 14	5.6	± 11	±14		V
Catput Voltago Civing	* O(P.P)	R <sub>S</sub> ≤10KΩ	± 10	± 13		± 9	± 13		V
Output Short Circuit Current	I <sub>SC</sub>			20			20		mA
Power Consumption	Pc	$V_O = 0V$		70	170		70	240	mW
Transient Response (Unity Gain)									
Rise Time	t <sub>RES</sub>	$V_1 = 20mV, R_L \ge 2K\Omega, C_L \le 100pF$		0.3			0.3		μs
Overshoot	os	$V_I = 20mV, R_L \ge 2K\Omega, C_L \le 100pF$		15			15		%
Slew Rate	SR	$V_I = 10V, R_L \ge 2K\Omega, C_L \le 100pF$		0.5			0.5		V/μs

#### **ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub>= +15V, V<sub>EE</sub> = -15V, NOTE 1, unless otherwise specified)

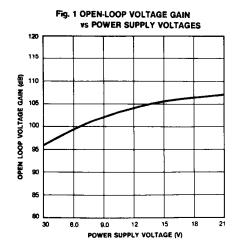
Characteristic	Cumbal	Took Conditions	LM1458A/AI			LM1458/I			l lmi4
Gilai actel IStic	Symbol Test Conditions	Min	Тур	Max	Min	Тур	Max	Unit	
Input Offset Voltage	V <sub>IO</sub>	R <sub>S</sub> ≤10KΩ			7.5			12	mV
Input Offset Current	I <sub>IO</sub>				300			400	nA
Input Bias Current	I <sub>BIAS</sub>				800			1000	nA
Large Signal Voltage Gain	$G_V$	$V_{O(P-P)} = \pm 10V, R_L \le 2.0K\Omega$	15			15			V/mV
Common Mode Rejection Ratio	CMRR	R <sub>S</sub> ≥10KΩ	70	90		70	90		dB
Power Supply Rejection Ratio	PSRR	R <sub>S</sub> ≥10KΩ	77	90		77	90		dB
Output Voltage Swing	V	$R_L = 10K\Omega$	± 12	± 14		± 11	± 14		V
Output Voltage Swing	$V_{O(P.P)}$	$R_L = 2K\Omega$	± 10	± 13		± 9	± 13		V
Input Voltage Range	$V_{I(R)}$		± 12			± 12			V

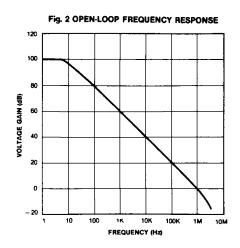
NOTE 1

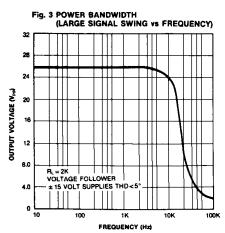
LM1458/A:  $0 \,^{\circ}\text{C} \leq T_{A} \leq 70 \,^{\circ}\text{C}$ LM1458I/AI:  $-25 \,^{\circ}\text{C} \leq T_{A} \leq +85 \,^{\circ}\text{C}$ 

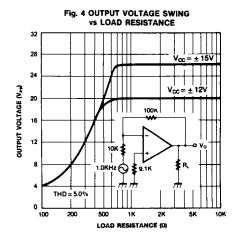


#### TYPICAL PERFORMANCE CHARACTERISTICS









#### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

#### **PRODUCT STATUS DEFINITIONS**

#### **Definition of Terms**

Datasheet Identification	Product Status	Definition	
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.	
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.	
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.	
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.	



# **LM148**

# Low Power Quad 741 Operational Amplifier

#### **Features**

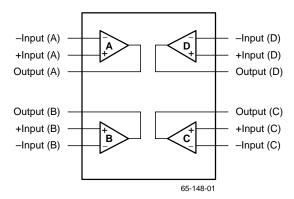
- 741 op amp operating characteristics
- Low supply current drain—0.6 mA/amplifier
- · Class AB output stage—no crossover distortion
- Pin compatible with the LM124
- Low input offset voltage—1.0 mV
- Low input offset current—4.0 nA
- Low input bias current—30 nA
- Unity gain bandwidth—1.0 MHz
- Channel Separation—120 dB
- · Input and output overload protection

# **Description**

The LM148 is a true quad 741. It consists of four independent high-gain, internally compensated, low-power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar 741 operational amplifier. In addition, the total supply current for all four amplifiers is comparable to the supply current of a single 741 type op amp. Other features include input offset currents and input bias currents which are much less than those of a standard 741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

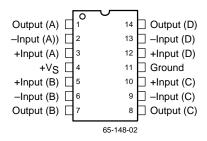
The LM148 can be used anywhere multiple 741 type amplifiers are being used and in applications where amplifier matching or high packing density is required.

# **Block Diagram**



LM148 PRODUCT SPECIFICATION

# **Pin Assignments**



# **Absolute Maximum Ratings**

Parameter	Min.	Max.	Unit	
Supply Voltage	-22	+22	V	
Differential Input Voltage		44	V	
Input Voltage <sup>1</sup>	-22	+22	V	
Output Short Circuit Duration <sup>2</sup>		Indefinite		
Storage Temperature Range	-65	+150	°C	
Operating Temperature Range	-55	+125	°C	
Lead Soldering Temperature (60 sec.)	+300°C			

#### Notes:

- 1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
- 2. Short circuit to ground on one amplifier only.

## **Thermal Characteristics**

Parameter	14-Lead Ceramic DIP	
Maximum Junction Temperature	+175°C	
Maximum PD TA < 50°C	1042 mW	
Thermal Resistance, θ <sub>JC</sub>	60°C/W	
Thermal Resistance, θJA	120°C/W	
For T <sub>A</sub> > 50°C derate at	8.33 mW/°C	

## **Electrical Characteristics**

(Vs =  $\pm 15$ V and TA = 25°C, unless otherwise noted)

Parameter	Test Conditions		Min.	Тур.	Max.	Unit
Input Offset Voltage	Rs ≤ 10KΩ		1.0	5.0	mV	
Input Offset Current			4.0	25	nA	
Input Bias Current				30	100	nA
Input Resistance (Differential Mode) <sup>1</sup>			0.8	2.5		MΩ
Supply Current, All Amplifiers	VS = ±15V			2.4	3.6	mA
Large Signal Voltage Gain	$V_S = \pm 15V, V_C$ $R_L \ge 2K\Omega$	OUT = ±10V,	50	160		V/mV
Channel Separation	F = 1 Hz 20 KH	-lz		120		dB
Unity Gain Bandwidth				1.0		MHz
Phase Margin					60	Degrees
Slew Rate					0.5	V/μS
Short Circuit Current				25		mA
The following specifications apply fo	r Vs = ±15V, -55°	°C ≤ TA ≤ +125°	C.			
Input Offset Voltage	Rs ≤ 10KΩ				6.0	mV
Input Offset Current					75	nA
Input Bias Current					325	nA
Large Signal Voltage Gain	$V_S = \pm 15V$ , $V_{OUT} = 10V$ , $R_L < 2K\Omega$		25			V/mV
Output Voltage Swing	VS = ±15V	RL = 10KΩ	±12	±13		V
		$R_L = 2K\Omega$	±10	±12		]
Input Voltage Range	Vs = ±15V		±12			V
Common Mode Rejection Ratio	Rs ≤ 10KΩ		70	90		dB
Power Supply Rejection Ratio	Rs ≤ 10KΩ		77	96		dB

<sup>1.</sup> Guaranteed by design but not tested.

LM148 PRODUCT SPECIFICATION

# **Typical Performance Characteristics**

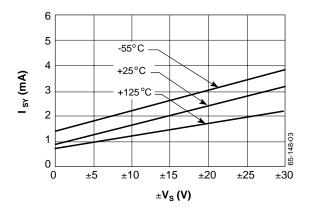


Figure 1. Supply Current vs. Supply Voltage

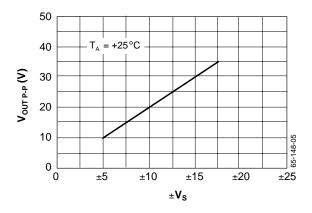


Figure 3. Output Voltage Swing vs. Supply Voltage

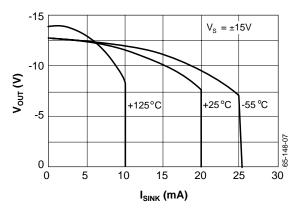


Figure 5. Negative Current Limit
Output Voltage vs. Output Sink Current

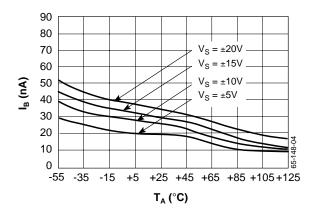


Figure 2. Input Bias Current vs. Temperature

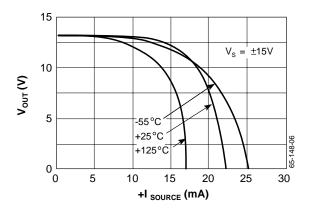


Figure 4. Positive Current Limit
Output Voltage vs. Output Source Current

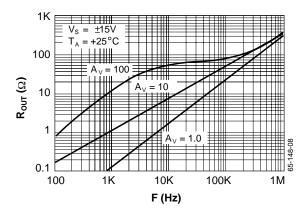


Figure 6. Output Impedance vs. Frequency

# **Typical Performance Characteristics** (continued)

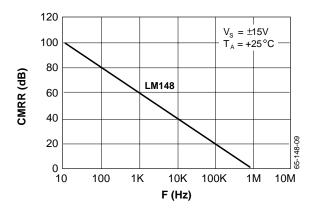


Figure 7. CMRR vs. Frequency

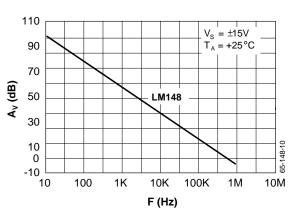


Figure 8. Open Loop Gain vs. Frequency

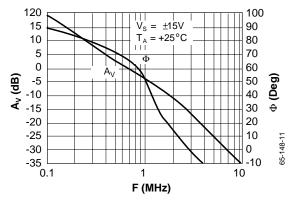


Figure 9. Gain, Phase vs. Frequency

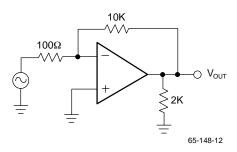


Figure 10. Gain, Phase Test Circuit

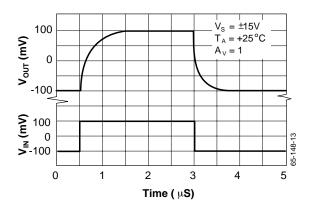


Figure 11. Small Signal Pulse Response Input, Output Voltage vs. Time

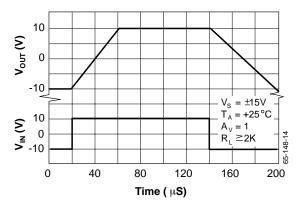


Figure 12. Large Signal Pulse Response Output Voltage vs. Time

LM148 PRODUCT SPECIFICATION

# **Typical Performance Characteristics** (continued)

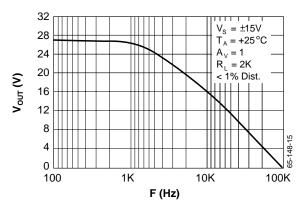


Figure 13. Undistorted Output Voltage Swing vs. Frequency

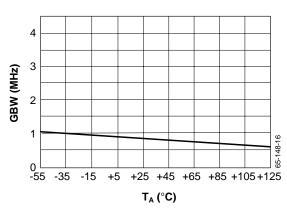


Figure 14. Gain Bandwidth Product vs. Temperature

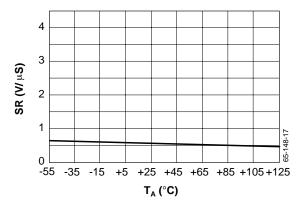


Figure 15. Slew Rate vs. Temperature

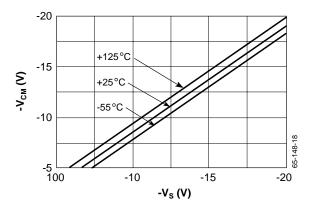


Figure 16. Negative Common Mode Input Voltage vs. Supply Voltage

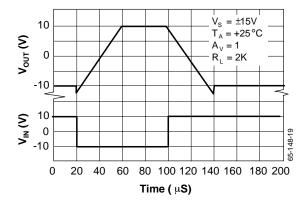


Figure 17. Inverting Large Signal Pulse Response Input, Output Voltage vs. Time

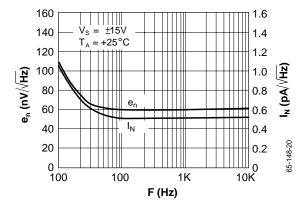


Figure 18. Input Noise Voltage, Current Densities vs. Frequency

# **Typical Performance Characteristics** (continued)

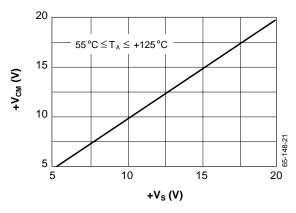


Figure 19. Positive Common Mode, Input Voltage vs. Supply Voltage

# **Typical Simulation**

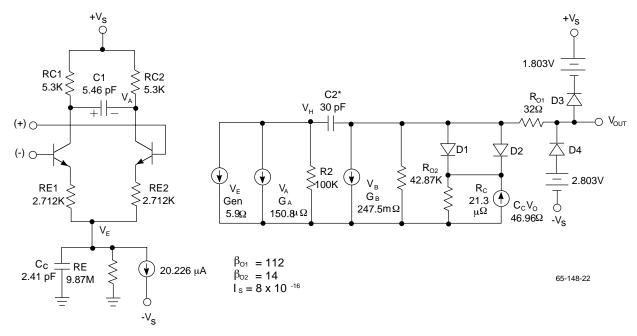


Figure 20. LM148 Macromodel for Computer Simulation

LM148 PRODUCT SPECIFICATION

## **Applications Discussion**

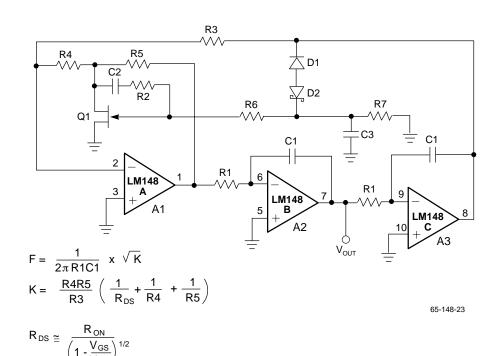
The LM148 low power quad operational amplifier exhibits performance comparable to the popular 741. Substitution can therefore be made with no change in circuit behavior.

The input characteristics of these devices allow differential voltages which exceed the supplies. Output phase will be correct as long as one of the inputs is within the operating common mode range. If both exceed the negative limit, the output will latch positive. Current limiting resistors should be used on the inputs in case voltages become excessive.

When capacitive loading becomes much greater than 100pF, a resistor should be placed between the output and feedback connection in order to reduce phase shift.

The LM148 is short circuit protected to ground and supplies continuously when only one of the four amplifiers is shorted. If multiple shorts occur simultaneously, the unit can be destroyed due to excessive power dissipation.

To assure stability and to minimize pickup, feedback resistors should be placed close to the input to maximize the feedback pole frequency (a function of input to ground capacitance). A good rule of thumb is that the feedback pole frequency should be 6 times the operating -3.0B frequency. If less, a lead capacitor should be placed between the output and input.



$$\begin{split} &F_{MAX} = 5.0 \text{ KHz}, \ THD \leq & 0.03\% \\ &R1 = 100 \text{K pot., } C1 = 0.0047 \, \mu\text{F}, \ C2 = 0.01 \, \mu\text{F}, \ C3 = 0.1 \, \mu\text{F}, \ R2 = R6 = R7 = 1 \text{M}, \ R3 = 5.1 \text{K}, \ R4 = 12 \Omega \, . \\ &R5 = 240 \, \Omega, \ Q1 = NS5102, \ D1 = 1 N914, \ D2 = 3.6 \text{V} \ \text{ avalanche diode (ex. LM103), } \ V_S = \pm 15 \text{V} \end{split}$$

A simpler version with some distortion degradation at high frequencies can be made by using A1 as a simple inverting amplifier, and by putting back to back zeners in feedback loop of A3.

Figure 21. One Decade Low Distortion Sinewave Generator

# **Applications Discussion** (continued)

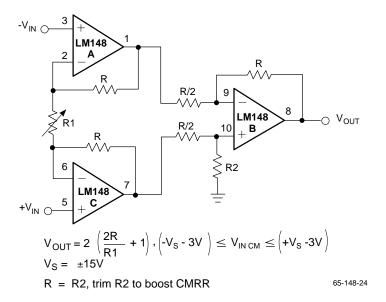


Figure 22. Low Cost Instrumentation Amplifier

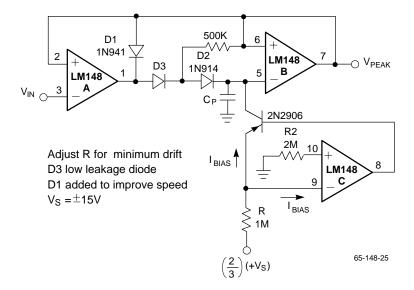


Figure 23. Low Voltage Peak Detector with Bias Current Compensation

LM148 PRODUCT SPECIFICATION

# **Applications Discussion** (continued)

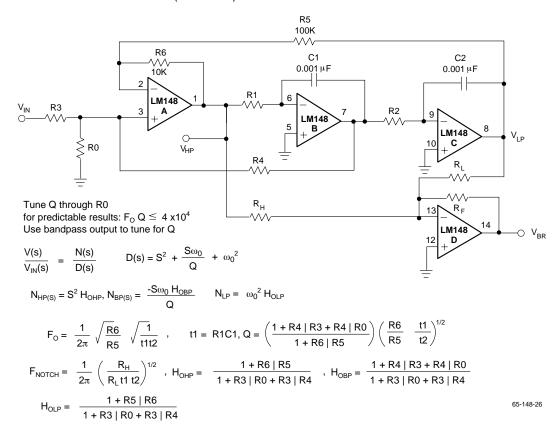
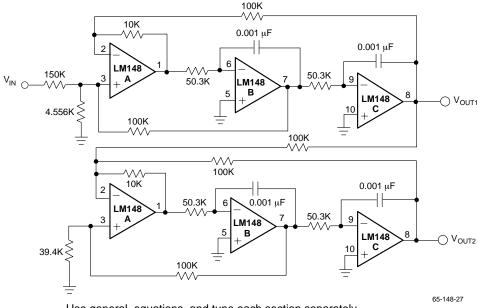


Figure 24. Universal State-Space Filter



Use general equations, and tune each section separately.

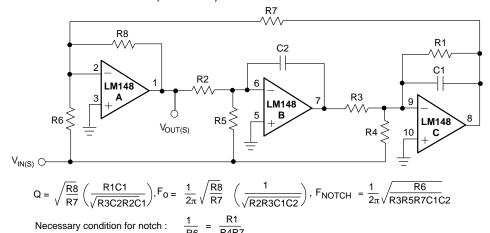
 $Q_{1st}$  Section = 0.541,  $Q_{2nd}$  Section = 1.306.

The response should have 0 dB peaking.

Figure 25. 1 KHz 4-Pole Butterworth Filter

# **Applications Discussion** (continued)

 $C1 = C2 = 0.001 \mu F$ .

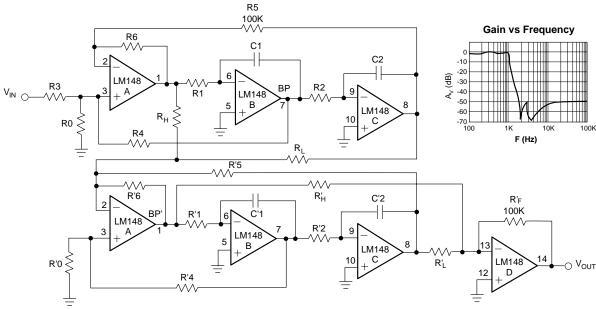


Examples:  $F_{NOTCH} = 3 \text{ kHz}$ , Q = 5, R1 = 270 K, R2 = R3 = 20 K, R4 = 27 K, R5 = 20 K, R6 = R8 = 10 K, R7 = 100 K.

Better noise performance than the state-space approach.

65-148-28

Figure 26. 3 Amplifier Bi-Quad Notch Filter



 $\rm F_C=1$  kHz,  $\rm F_S=2$  kHz,  $\rm F_P=0.543.~F_Z=2.14,~Q=0.841,~F'_P=0.987,~F'_Z=4.92.~Q'=4.403$  normalized to ripple BW.

$$F_{P} = -\frac{1}{2^{T}}\sqrt{\frac{R6}{R5}} - \left(\frac{1}{t}\right), \\ F_{Z} = -\frac{1}{2^{T}}\sqrt{\frac{R_{H}}{R_{L}}}\left(\frac{1}{t}\right), \\ Q = -\frac{1 + R4/R3 + R4/R0}{1 + R6/R5} - x - \sqrt{\frac{R6}{R5}} - x - \sqrt{\frac{R'6}{R'5}} - x - \frac{1 + R'4/R'0}{1 + R'6/R'5 + R'6/R_{P}} - \frac{1}{R'5} - \frac{1}$$

$$R_{P} = \frac{R_{H} R_{L}}{R_{H} + R_{L}}$$

Use the B'P outputs to tune Q, Q', tune the 2 sections separately. R1 = R2 = 92.6K, R3 = R4 = R5 = 100K, R6 = 10K, R0 = 107.8K,  $R_L$  = 100K,  $R_H$  = 155.1K, R'1 = R'2 = 50.9K, R'4 = R'5 = 100K, R'6 = 10K, R'0 = 5.78K,  $R_L$  = 100K,  $R_H$  = 248.12K,  $R_F$  = 100K.

65-148-29

All capacitors are  $0.001 \mu \text{F}.$ 

Figure 27. 4th Order 1 KHz Elliptic Filter (4 Poles, 4 Zeros)

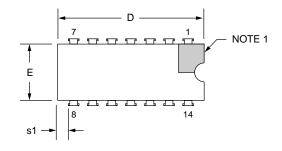
LM148 PRODUCT SPECIFICATION

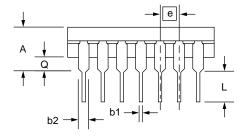
LM148 PRODUCT SPECIFICATION

## **Mechanical Dimensions**

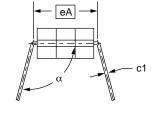
## 14-Pin Ceramic DIP

Symbol	Inc	Inches		Millimeters	
Symbol	Min.	Max.	Min.	Max.	Notes
Α	_	.200	_	5.08	
b1	.014	.023	.36	.58	8
b2	.045	.065	1.14	1.65	2
c1	.008	.015	.20	.38	8
D		.785		19.94	4
Е	.220	.310	5.59	7.87	4
е	.100 BSC		2.54	BSC	5, 9
eA	.300	BSC	7.62	BSC	7
L	.125	.200	3.18	5.08	
Q	.015	.060	.38	1.52	3
s1	.005	_	.13	_	6
α	90°	105°	90°	105°	





- Index area: a notch or a pin one identification mark shall be located adjacent to pin one. The manufacturer's identification shall not be used as pin one identification mark.
- 2. The minimum limit for dimension "b2" may be .023 (.58mm) for leads number 1, 7, 8 and 14 only.
- 3. Dimension "Q" shall be measured from the seating plane to the base plane.
- 4. This dimension allows for off-center lid, meniscus and glass overrun.
- The basic pin spacing is .100 (2.54mm) between centerlines. Each pin centerline shall be located within ±.010 (.25mm) of its exact longitudinal position relative to pins 1 and 14.
- 6. Applies to all four corners (leads number 1, 7, 8, and 14).
- "eA" shall be measured at the center of the lead bends or at the centerline of the leads when "a" is 90°.
- 8. All leads Increase maximum limit by .003 (.08mm) measured at the center of the flat, when lead finish applied.
- 9. Twelve spaces.



LM148 PRODUCT SPECIFICATION

# **Ordering Information**

Part Number	Package	Operating Temperature Range
LM148D	14-Lead Ceramic DIP	-55°C to +125°C
LM148D/883B	14-Lead Ceramic DIP	-55°C to +125°C

#### Note:

1. 883B suffix denotes Mil-Std-883, Level B processing

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com



# LM1851

# **Ground Fault Interrupter**

## **Features**

- No potentiometer required
- · Direct interface to SCR
- Supply voltage derived from AC line—26V shunt
- · Adjustable sensitivity

- · Grounded neutral fault detection
- Meets UL943 standards
- 450 µA quiescent current
- · Ideal for 120V or 220V systems

# **Description**

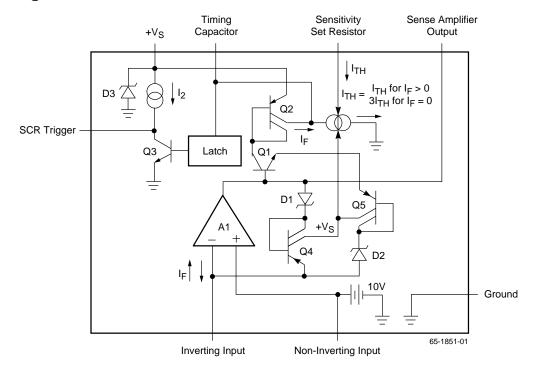
The LM1851 is a controller for AC outlet ground fault interrupters. These devices detect hazardous grounding conditions (example: a pool of water and electrical equipment connected to opposite phases of the AC line) in consumer and industrial environments. The output of the IC triggers an external SCR, which in turn opens a relay circuit breaker to prevent a harmful or lethal shock.

Full advantage of the U.S. UL943 timing specification is taken to ensure maximum immunity to false triggering due

to line noise. A special feature is found in circuitry that rapidly resets the integrating timing capacitor in the event that noise pulses introduce unwanted charging currents. Also, flip-flop is included that ensures firing of even a slow circuit breaker relay on either half-cycle of the line voltage when external full wave rectification is used.

The application circuit can be configured to detect both normal faults (hot wire to ground) and grounded neutral faults.

# **Block Diagram**



LM1851 PRODUCT SPECIFICATION

# **Functional Description**

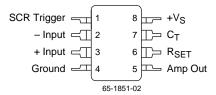
The voltage at the supply pin is clamped to +26V by the internal shunt regulator D3. This shunt regulator also generates an artificial ground voltage for the noninverting input of A1 (shown as a +10V source). A1, Q1, and Q2 act a a current mirror for fault current signals (which are derived from an external transformer). When a fault signal is present, the mirrored current charges the external timing capacitor until its voltage exceeds the latch trigger threshold (typically 17.5V). When then this threshold is exceeded, the latch engages and Q3 turns off, allowing I2 to drive the SCR connected to pin 1.

Extra Circuitry in the feedback path of A1 works with the switched current source I<sub>1</sub> to remove any charge on C<sub>T</sub> induced by noise in the transformer. If no fault current is

present, then I<sub>1</sub> discharges C<sub>T</sub> with a current equal to 3 I<sub>TH</sub>, where I<sub>TH</sub> is the value of current set by the external R<sub>SET</sub> resistor. If fault signals are present at the input of A<sub>1</sub> (which is held at virtual ground, +10V), one of the two current mirrors in the feedback path of A<sub>1</sub> (Q<sub>4</sub> and Q<sub>5</sub>) will become active, depending on which half-cycle the fault occurs. This action will raise the voltage at V<sub>S</sub>, switching I<sub>1</sub> to a value equal to I<sub>TH</sub>, and reducing the discharge rate of C<sub>T</sub> to better allow fault currents to charge it.

Notice that ITH discharges CT during both half-cycles of the line, while IF only charges CT during the half-cycle in which IF exits pin 2 (since Q1 will only carry fault current in one direction). Thus, during one half-cycle, IF-ITH charges CT, while during the other half-cycle ITH discharges it.

## **Pin Assignments**



## **Definition of Terms**

## **Normal Fault**

An unintentional electrical path, R<sub>B</sub>, between the load terminal of the hot line and the ground, as shown by the dashed lines in Figure 1.

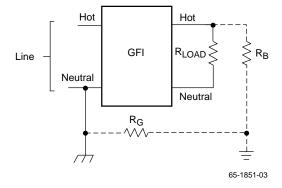


Figure 1. Normal Fault

## **Grounded Neutral Fault**

An unintentional electrical path between the load terminal of the neutral line and the ground, as shown by the dashed lines in Figure 2.

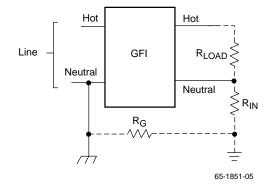


Figure 2. Grounded Neutral Fault

## **Normal Fault Plus Grounded Neutral Fault**

The combination of the normal fault and the grounded neutral fault, as shown by the dashed lines in Figure 3.

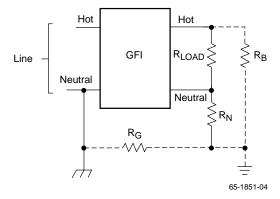


Figure 3. Normal Fault Plus Grounded Neutral Fault

# **Absolute Maximum Ratings**

Parameter	Conditions	Min	Max	Units
Supply Current			19	mA
Power Dissipation			570	mW
Operating Temperature		-40	70	°C
Lead Soldering Temperature	SOIC, 10 seconds		260	°C
	DIP, 60 seconds		300	°C

# **Thermal Characteristics**

Parameter	Conditions	Min	Max	Units
Maximum Junction Temperature			125	°C
Maximum PDTA < 50°C	DIP		468	mW
	SOIC		300	
Thermal Resistance, θJA	DIP		160	°C/W
	SOIC		240	
For TA > 50°C, derate at	DIP		6.25	mW/°C
	SOIC		4.17	

LM1851 PRODUCT SPECIFICATION

## **DC Electrical Characteristics**

 $(T_A = +25^{\circ}C, I_{SHUNT} = 5 mA)$ 

Parameters	Test Conditions	Min	Тур	Max	Units
Power Supply Shunt Regulator Voltage	Pin 8, Average Value	22	26	30	V
Latch Trigger Voltage	Pin 7	15	17.5	20	V
Sensitivity Set Voltage	Pin 8 to Pin 6	6	7	8.2	V
Output Drive Current	Pin 1 With Fault	0.5	1	2.4	mA
Output Saturation Voltage	Pin 1 Without Fault		100	240	mV
Output Saturation Resistance	Pin 1 Without Fault		100		Ω
Output External Current Sinking Capability <sup>1</sup>	Pin 1 Without Fault, VPIN1 Held to 0.3V	2	5		mA
Noise Integration Sink Current Ratio	Pin 7, Ratio of Discharge Currents Between No Fault Fault and Fault Conditions	2.0	2.8	3.6	μΑ/μΑ

## Notes:

# **AC Electrical Characteristics**

 $(TA = +25^{\circ}C, ISHUNT = 5 mA)$ 

Parameters	Conditions	Min	Тур	Max	Units
Normal Fault Current Sensitivity <sup>2</sup>	See Figure 9	3	5	7	mA
Normal Fault Trip Time <sup>1</sup>	500Ω Fault, see Figure 10		18		mS
Normal Fault With Grounded	500Ω Normal Fault		18		mS
Neutral Fault Trip Time <sup>1</sup>	2Ω Neutral, see Figure 10				

- 1. Average of 10 trials.
- 2. Required UL sensitivity tolerance is such that external trimming of LM1851 sensitivity is necessary.

<sup>1.</sup> This external applied current is in addition to the internal "output drive current" source.

# **Typical Performance Characteristics** (TA = +25°C)

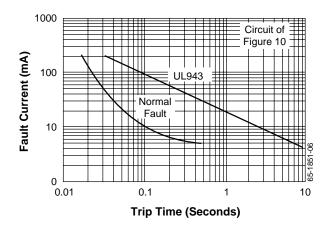


Figure 4. Average Trip Time vs. Fault Current

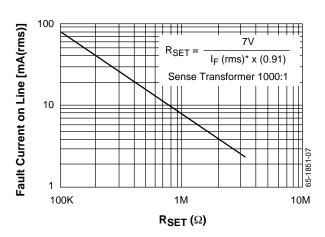


Figure 5. Normal Fault Current Threshold vs. RSET

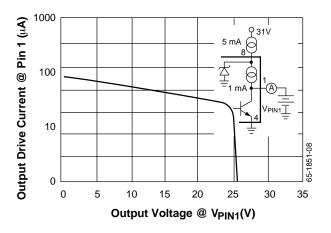


Figure 6. Output Drive Current vs. Output Voltage

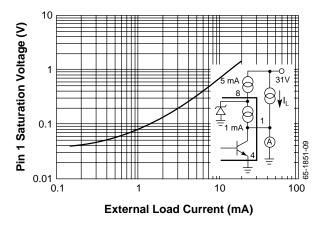


Figure 7. Pin 1 Saturation Voltage vs. External Load Current, IL

LM1851 PRODUCT SPECIFICATION

## **Applications Discussion**

A typical ground fault interrupter circuit is shown in Figure 10. It is designed to operate on 120 VAC line voltage with 5 mA normal fault sensitivity.

A full-wave rectifier bridge and a 15k/2W resistor are used to supply the dc power required by the IC. A 1  $\mu F$  capacitor at pin 8 is used to filter the ripple of the supply voltage and is also connected across the SCR to allow firing of the SCR on either half-cycle. When a fault causes the SCR to trigger, the circuit breaker is energized and line voltage is removed from the load.

At this time no fault current flows and the CT discharge current increases from ITH to 3ITH (see Block Diagram). This quickly resets both the timing capacitor and the output latch. The circuit breaker can be reset and the line voltage again supplied to the load, assuming the fault has been removed. A 1000:1 sense transformer is used to detect the normal fault. The fault current, which is basically the difference current between the got and neutral lines, is stepped down by 1000 and fed into the input pin of the operational amplifier through a 10  $\mu F$  capacitor. The 0.0033  $\mu F$  capacitor between pin 2 and pin 3 and the 200 pF between pins 3 and 4 are added to obtain better noise immunity. The normal fault sensitivity is determined by the timing capacitor discharging current, ITH. ITH can be calculated by:

$$I_{TH} = \frac{7V}{R_{SFT}} \div 2 \tag{1}$$

At the decision point, the average fault current just equals the threshold current, ITH.

$$I_{TH} = \frac{I_F(rms)}{2} \times 0.91 \tag{2}$$

Where IF(rms) is the rms input fault current to the operational amplifier and the factor of 2 is due to the fact that IF charges the timing capacitor only during one half-cycle, while ITH discharges the capacitor continuously. The factor 0.91 converts the rms value to an average value. Combining equations (1) and (2) we have:

$$R_{SET} = \frac{7V}{I_F(rms) \times 0.91} \tag{3}$$

For example, to obtain 5 mA(rms) sensitivity for the circuit in Figure 7 we have:

$$R_{SET} = \frac{7V}{\frac{5 \text{ mA} \times 0.91}{1000}} = 1.5 \text{M}\Omega$$
 (4)

The correct value for RSET can also be determined from the characteristic curve that plots equation (3). Note that this is an approximate calculation; the exact value of RSET depends on the specific sense transformer used and LM1851 tolerances. Inasmuch as UL943 specifies a sensitivity "window" of 4 mA to 6mA, provision should be made to adjust RSET with a potentiometer.

Independent of setting sensitivity, the desired integration time can be obtained through proper selection of the timing capacitor, C<sub>T</sub>. Due to the large number of variables involved, proper selection of C<sub>T</sub> is best done empirically. The following design example should only be used as a guideline.

Assume the goal is to meet UL943 timing requirements. Also assume that worst case timing occurs during GFI start-up (S1 closure) with both a heavy normal fault and a  $2\Omega$  grounded neutral fault present. This situation is shown diagrammatically in Figure 8.

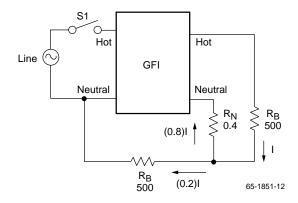


Figure 8.

UL943 specifies ≤25 ms average trip time under these conditions. Calculation of C<sub>T</sub> based upon charging currents due to normal fault only is as follows:

- Start with a ≤25 ms specification. Subtract 3 ms GFI turn-on time (15k and 1 μF). Subtract 8 ms potential loss of one half-cycle due to fault current sense of halfcycles only.
- Subtract 4 ms time required to open a sluggish circuit breaker.
- This gives a total ≤10 ms maximum integration time that could be allowed.
- 4. To generate 8 ms value of integration time that accommodates component tolerances and other variables:

$$C_{T} = \frac{1 \times T}{V} \tag{5}$$

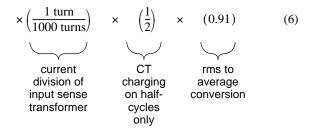
where:

T = integration timeV = threshold voltage

V = threshold voltage

I = average fault current into CT

$$I = \left(\frac{120 \text{ V}_{AC}(rms)}{R_B}\right) \qquad \left(\frac{RN}{RG + RN}\right)$$
 heavy fault current generated (swamps ITH) portion of fault current shunted around GFI



therefore:

$$\begin{split} C_{\mathrm{T}} &= \frac{\left[ \left( \frac{120}{500} \right) \times \left( \frac{0.4}{1.6 + 0.4} \right) \times \left( \frac{1}{1000} \right) \times \left( \frac{1}{2} \right) \times (0.91) \right]}{17.5} \times 0.008 \\ C_{\mathrm{T}} &= 0.01 \ \mu \mathrm{F} \end{split}$$

In practice, the actual value of C<sub>T</sub> will have to be modified to include the effects of the neutral loop upon the net charging current. The effect of neutral loop induced currents is difficult to quantize, but typically they sum with normal fault currents, thus allowing a larger value of C<sub>T</sub>.

For UL943 requirements,  $0.015 \mu F$  has been found to be the best compromise between timing and noise.

For those GFI standards not requiring grounded neutral detection, a still larger value capacity can be used and better noise immunity obtained.

The larger capacitor can be accommodated because  $R_N$  and  $R_G$  are not present, allowing the full fault current, I, to enter the GFI.

In Figure 10, grounded neutral detection is accomplished by feeding the neutral coil with 120 Hz energy continuously and allowing some of the energy to couple into the sense transformer during conditions of neutral fault.

Transformers may be obtained from Magnetic Metals, Inc., 21st Street and Hayes Street, Camden, NJ 08101— (609) 964-7842.

LM1851 PRODUCT SPECIFICATION

# **Application Circuits**

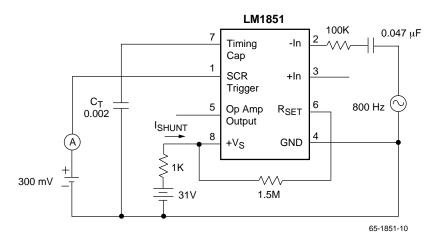


Figure 9. Normal Fault Sensitivity Test Circuit

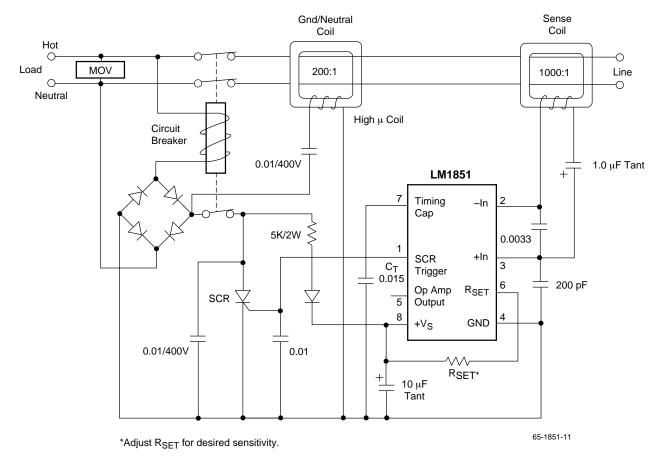
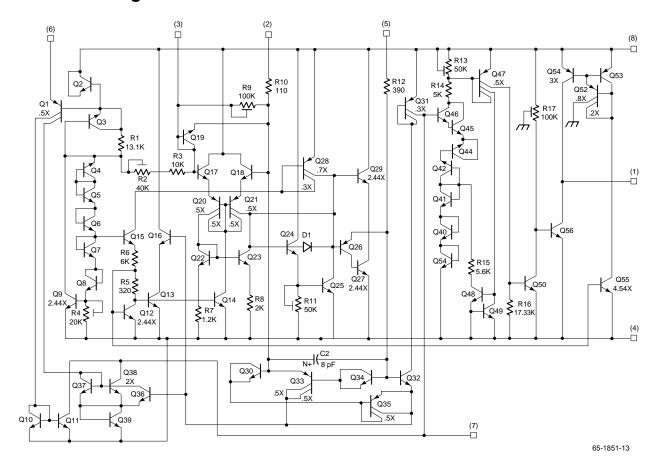


Figure 10. 120 Hz Neutral Transformer Application

# **Schematic Diagram**



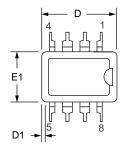
LM1851 PRODUCT SPECIFICATION

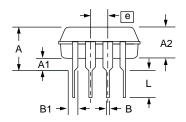
# **Mechanical Dimensions**

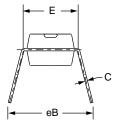
# 8-Lead Plastic DIP Package

Cumbal	Inc	hes	Millimeters		Notes
Symbol	Min.	Max.	Min.	Max.	Notes
А	_	.210	_	5.33	
A1	.015	_	.38	_	
A2	.115	.195	2.93	4.95	
В	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
С	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	_	.13	_	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
е	.100 BSC		2.54	BSC	
еВ	_	.430	_	10.92	
L	.115	.160	2.92	4.06	
N	8°		8	3°	5

- 1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- 2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
- 3. Terminal numbers are for reference only.
- 4. "C" dimension does not include solder finish thickness.
- 5. Symbol "N" is the maximum number of terminals.





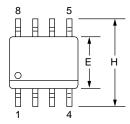


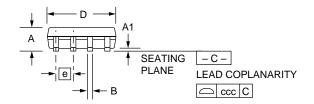
# **Mechanical Dimensions** (continued)

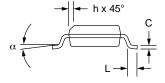
## 8-Lead Plastic SOIC Package

Symbol	Inches		Millimeters		Notes
Symbol	Min.	Max.	Min.	Max.	Notes
Α	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
В	.013	.020	0.33	0.51	
С	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
Е	.150	.158	3.81	4.01	2
е	.050	BSC	1.27 BSC		
Н	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	_	.004	_	0.10	

- 1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
- "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
- 3. "L" is the length of terminal for soldering to a substrate.
- 4. Terminal numbers are shown for reference only.
- 5. "C" dimension does not include solder finish thickness.
- 6. Symbol "N" is the maximum number of terminals.







LM1851 PRODUCT SPECIFICATION

# **Ordering Information**

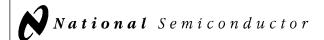
Part Number Package		Operating Temperature Range
LM1851AN	8-lead Plastic DIP	-40°C to +70°C
RV4145M	8-lead Plastic SOIC	-40°C to +70°C

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com



# LM1882•54ACT/74ACT715 LM1882-R•54ACT/74ACT715-R Programmable Video Sync Generator

## **General Description**

The 'ACT715/LM1882 and 'ACT715-R/LM1882-R are 20-pin TTL-input compatible devices capable of generating Horizontal, Vertical and Composite Sync and Blank signals for televisions and monitors. All pulse widths are completely definable by the user. The devices are capable of generating signals for both interlaced and noninterlaced modes of operation. Equalization and serration pulses can be introduced into the Composite Sync signal when needed.

Four additional signals can also be made available when Composite Sync or Blank are used. These signals can be used to generate horizontal or vertical gating pulses, cursor position or vertical Interrupt signal.

These devices make no assumptions concerning the system architecture. Line rate and field/frame rate are all a function of the values programmed into the data registers, the status register, and the input clock frequency.

The 'ACT715/LM1882 is mask programmed to default to a Clock Disable state. Bit 10 of the Status Register, Register 0, defaults to a logic "0". This facilitates (re)programming before operation.

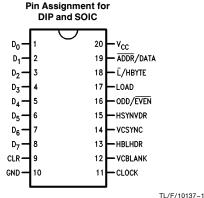
The 'ACT715-R/LM1882-R is the same as the 'ACT715/LM1882 in all respects except that the

'ACT715-R/LM1882-R is mask programmed to default to a Clock Enabled state. Bit 10 of the Status Register defaults to a logic "1". Although completely (re)programmable, the 'ACT715-R/LM1882-R version is better suited for applications using the default 14.31818 MHz RS-170 register values. This feature allows power-up directly into operation, following a single CLEAR pulse.

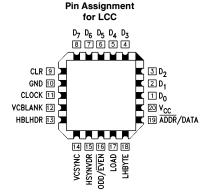
#### **Features**

- Maximum Input Clock Frequency > 130 MHz
- Interlaced and non-interlaced formats available
- Separate or composite horizontal and vertical Sync and Blank signals available
- Complete control of pulse width via register programming
- All inputs are TTL compatible
- 8 mA drive on all outputs
- Default RS170/NTSC values mask programmed into registers
- 4 KV minimum ESD immunity
- 'ACT715-R/LM1882-R is mask programmed to default to a Clock Enable state for easier start-up into 14.31818 MHz RS170 timing

## **Connection Diagrams**



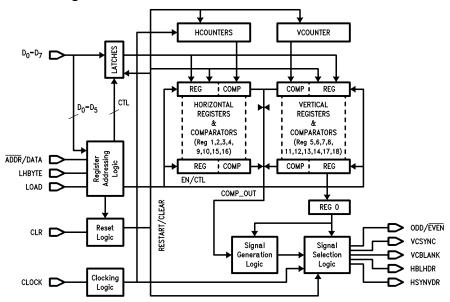
Order Number LM1882CN or LM1882CM For Default RS-170, Order Number LM1882-RCN or LM1882-RCM



TL/F/10137-2

TRI-STATE® is a registered trademark of National Semiconductor Corporation. FACT™ is a trademark of National Semiconductor Corporation.

## **Logic Block Diagram**



TL/F/10137-3

## **Pin Description**

There are a Total of 13 inputs and 5 outputs on the 'ACT715/LM1882.

**Data Inputs D0-D7:** The Data Input pins connect to the Address Register and the Data Input Register.

ADDR/DATA: The ADDR/DATA signal is latched into the device on the falling edge of the LOAD signal. The signal determines if an address (0) or data (1) is present on the data bus

**L/HBYTE:** The L/HBYTE signal is latched into the device on the falling edge of the LOAD signal. The signal determines if data will be read into the 8 LSB's (0) or the 4 MSB's (1) of the Data Registers. A 1 on this pin when an ADDR/DATA is a 0 enables Auto-Load Mode.

**LOAD:** The LOAD control pin loads data into the Address or Data Registers on the rising edge.  $\overline{\text{ADDR}}/\text{DATA}$  and  $\overline{\text{L}}/\text{HBYTE}$  data is loaded into the device on the falling edge of the LOAD. The LOAD pin has been implemented as a Schmitt trigger input for better noise immunity.

**CLOCK:** System CLOCK input from which all timing is derived. The clock pin has been implemented as a Schmitt trigger for better noise immunity. The CLOCK and the LOAD signal are asynchronous and independent. Output state changes occur on the falling edge of CLOCK.

**CLR:** The CLEAR pin is an asynchronous input that initializes the device when it is HIGH. Initialization consists of setting all registers to their mask programmed values, and initializing all counters, comparators and registers. The CLEAR pin has been implemented as a Schmitt trigger for better noise immunity. A CLEAR pulse should be asserted by the user immediately after power-up to ensure proper initialization of the registers—even if the user plans to (re)program the device.

**Note:** A CLEAR pulse will disable the CLOCK on the 'ACT715/LM1882 and will enable the CLOCK on the 'ACT715-R/LM1882-R.

**ODD/EVEN:** Output that identifies if display is in odd (HIGH) or even (LOW) field of interlace when device is in interlaced mode of operation. In noninterlaced mode of operation this output is always HIGH. Data can be serially scanned out on this pin during Scan Mode.

VCSYNC: Outputs Vertical or Composite Sync signal based on value of the Status Register. Equalization and Serration pulses will (if enabled) be output on the VCSYNC signal in composite mode only.

**VCBLANK:** Outputs Vertical or Composite Blanking signal based on value of the Status Register.

**HBLHDR:** Outputs Horizontal Blanking signal, Horizontal Gating signal or Cursor Position based on value of the Status Register.

**HSYNVDR:** Outputs Horizontal Sync signal, Vertical Gating signal or Vertical Interrupt signal based on value of Status Register.

## **Register Description**

All of the data registers are 12 bits wide. Width's of all pulses are defined by specifying the start count and end count of all pulses. Horizontal pulses are specified with-respect-to the number of clock pulses per line and vertical pulses are specified with-respect-to the number of lines per frame.

#### **REGO—STATUS REGISTER**

The Status Register controls the mode of operation, the signals that are output and the polarity of these outputs. The default value for the Status Register is 0 (000 Hex) for the 'ACT715/LM1882 and is "512" (200 Hex) for the 'ACT715-R/LM1882-R.

## Register Description (Continued)

Bits 0-2

B <sub>2</sub>	В1	В	VCBLANK	VCSYNC	HBLHDR	HSYNVDR
0	0	0	CBLANK	CSYNC	HGATE	VGATE
(DEFAULT)						
0	0	1	VBLANK	CSYNC	HBLANK	VGATE
0	1	0	CBLANK	VSYNC	<b>HGATE</b>	HSYNC
0	1	1	VBLANK	VSYNC	HBLANK	HSYNC
1	0	0	CBLANK	CSYNC	CURSOR	VINT
1	0	1	VBLANK	CSYNC	HBLANK	VINT
1	1	0	CBLANK	VSYNC	CURSOR	HSYNC
1	1	1	VBLANK	VSYNC	HBLANK	HSYNC

Bits 3-4

B <sub>4</sub>	В3	Mode of Operation
0	0	Interlaced Double Serration and
(DEF	AULT)	Equalization
0	1	Non Interlaced Double Serration
1	0	Illegal State
1	1	Non Interlaced Single Serration and Equalization

Double Equalization and Serration mode will output equalization and serration pulses at twice the HSYNC frequency (i.e., 2 equalization or serration pulses for every HSYNC pulse). Single Equalization and Serration mode will output an equalization or serration pulse for every HSYNC pulse. In Interlaced mode equalization and serration pulses will be output during the VBLANK period of every odd and even field. Interlaced Single Equalization and Serration mode is not possible with this part.

#### Bits 5-8

Bits 5 through 8 control the polarity of the outputs. A value of zero in these bit locations indicates an output pulse active LOW. A value of 1 indicates an active HIGH pulse.

B5- VCBLANK Polarity

**B6— VCSYNC Polarity** 

B7— HBLHDR Polarity

B8- HSYNVDR Polarity

#### Bits 9-11

Bits 9 through 11 enable several different features of the device.

B9— Enable Equalization/Serration Pulses (0)
 Disable Equalization/Serration Pulses (1)

B10— Disable System Clock (0) Enable System Clock (1)

Default values for B10 are "0" in the 'ACT715/LM1882 and "1" in the 'ACT715-R/LM1882-R.

B11— Disable Counter Test Mode (0) Enable Counter Test Mode (1)

This bit is not intended for the user but is for internal testing only.

#### HORIZONTAL INTERVAL REGISTERS

The Horizontal Interval Registers determine the number of clock cycles per line and the characteristics of the Horizontal Sync and Blank pulses.

REG1— Horizontal Front Porch

REG2— Horizontal Sync Pulse End Time

REG3— Horizontal Blanking Width

REG4— Horizontal Interval Width # of Clocks per Line

#### **VERTICAL INTERVAL REGISTERS**

The Vertical Interval Registers determine the number of lines per frame, and the characteristics of the Vertical Blank and Sync Pulses.

REG5— Vertical Front Porch

REG6— Vertical Sync Pulse End Time

REG7— Vertical Blanking Width

REG8— Vertical Interval Width # of Lines per Frame

# EQUALIZATION AND SERRATION PULSE SPECIFICATION REGISTERS

These registers determine the width of equalization and serration pulses and the vertical interval over which they occur.

REG 9— Equalization Pulse Width End Time

REG10— Serration Pulse Width End Time

REG11— Equalization/Serration Pulse Vertical Interval Start Time

REG12— Equalization/Serration Pulse Vertical Interval End Time

#### VERTICAL INTERRUPT SPECIFICATION REGISTERS

These Registers determine the width of the Vertical Interrupt signal if used.

REG13— Vertical Interrupt Activate Time

REG14— Vertical Interrupt Deactivate Time

#### **CURSOR LOCATION REGISTERS**

These 4 registers determine the cursor position location, or they generate separate Horizontal and Vertical Gating signals

REG15— Horizontal Cursor Position Start Time

REG16— Horizontal Cursor Position End Time

REG17— Vertical Cursor Position Start Time

REG18— Vertical Cursor Position End Time

## **Signal Specification**

# HORIZONTAL SYNC AND BLANK SPECIFICATIONS

All horizontal signals are defined by a start and end time. The start and end times are specified in number of clock cycles per line. The start of the horizontal line is considered pulse 1 not 0. All values of the horizontal timing registers are referenced to the falling edge of the Horizontal Blank signal (see *Figure 1*). Since the first CLOCK edge, CLOCK #1, causes the first falling edge of the Horizontal Blank reference pulse, edges referenced to this first Horizontal edge are n + 1 CLOCKs away, where "n" is the width of the timing in question. Registers 1, 2, and 3 are programmed in this manner. The horizontal counters start at 1 and count until HMAX. The value of HMAX must be divisible by 2. This

## Signal Specification (Continued)

# SYSCK HMAX REG3 HSYNC HEQP REG1 REG2 HSERP HMAX/2

FIGURE 1. Horizontal Waveform Specification

limitation is imposed because during interlace operation this value is internally divided by 2 in order to generate serration and equalization pulses at 2  $\times$  the horizontal frequency. Horizontal signals will change on the falling edge of the CLOCK signal. Signal specifications are shown below.

 $\begin{array}{lll} \mbox{Horizontal Period (HPER)} &= \mbox{REG(4)} \times \mbox{ckper} \\ \mbox{Horizontal Blanking Width} &= \mbox{[REG(3)} - 1] \times \mbox{ckper} \\ \mbox{Horizontal Sync Width} &= \mbox{[REG(2)} - \mbox{REG(1)} \times \mbox{ckper} \\ \mbox{Horizontal Front Porch} &= \mbox{[REG(1)} - 1] \times \mbox{ckper} \end{array}$ 

#### **VERTICAL SYNC AND BLANK SPECIFICATION**

All vertical signals are defined in terms of number of lines per frame. This is true in both interlaced and noninterlaced modes of operation. Care must be taken to not specify the Vertical Registers in terms of lines per field. Since the first CLOCK edge, CLOCK #1, causes the first falling edge of the Vertical Blank (first Horizontal Blank) reference pulse, edges referenced to this first edge are n + 1 lines away. where "n" is the width of the timing in question. Registers 5, 6, and 7 are programmed in this manner. Also, in the interlaced mode, vertical timing is based on half-lines. Therefore registers 5 6 and 7 must contain a value twice the total horizontal (odd and even) plus 1 (as described above). In non-interlaced mode, all vertical timing is based on wholelines. Register 8 is always based on whole-lines and does not add 1 for the first clock. The vertical counter starts at the value of 1 and counts until the value of VMAX. No restrictions exist on the values placed in the vertical registers. Vertical Blank will change on the leading edge of HBLANK. Vertical Sync will change on the leading edge of HSYNC. (See Figure 2A.)

Vertical Frame Period (VPER) = REG(8)  $\times$  hper Vertical Field Period (VPER/n) = REG(8)  $\times$  hper/n Vertical Blanking Width = [REG(7) - 1]  $\times$  hper/n Vertical Syncing Width = [REG(6) - REG(5)]  $\times$  hper/n Vertical Front Porch = [REG(5) - 1]  $\times$  hper/n where n = 1 for noninterlaced n = 2 for interlaced

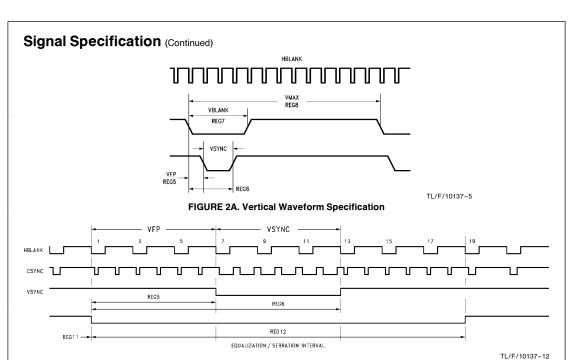
TL/F/10137-4

#### **COMPOSITE SYNC AND BLANK SPECIFICATION**

Composite Sync and Blank signals are created by logically ANDing (ORing) the active LOW (HIGH) signals of the corresponding vertical and horizontal components of these signals. The Composite Sync signal may also include serration and/or equalization pulses. The Serration pulse interval occurs in place of the Vertical Sync interval. Equalization pulses occur preceding and/or following the Serration pulses. The width and location of these pulses can be programmed through the registers shown below. (See Figure 2B.)

```
\label{eq:horizontal} \begin{aligned} \text{Horizontal Equalization PW} &= [\text{REG}(9) - \text{REG}(1)] \times \text{ckper} \\ &= \text{REG } 9 = (\text{HFP}) + (\text{HEQP}) \\ &+ 1 \end{aligned} \text{Horizontal Serration PW} &= [\text{REG}(4)/n + \text{REG}(1) - \text{REG}(10)] \times \text{ckper} \\ \text{REG } 10 = (\text{HFP}) + (\text{HPER}/2) - (\text{HSERR}) + 1 \end{aligned}
```

Where n=1 for noninterlaced single serration/equalization n=2 for noninterlaced double serration/equalization n=2 for interlaced operation



## FIGURE 2B. Equalization/Serration Interval Programming

#### HORIZONTAL AND VERTICAL GATING SIGNALS

Horizontal Drive and Vertical Drive outputs can be utilized as general purpose Gating Signals. Horizontal and Vertical Gating Signals are available for use when Composite Sync and Blank signals are selected and the value of Bit 2 of the Status Register is 0. The Vertical Gating signal will change in the same manner as that specified for the Vertical Blank.

Horizontal Gating Signal Width = [REG(16) - REG(15)]  $\times$  ckper

 $\begin{tabular}{ll} \mbox{Vertical Gating Signal Width} & = [\mbox{REG(18)} - \mbox{REG(17)}] \times \\ & \mbox{hper} \end{tabular}$ 

## **CURSOR POSITION AND VERTICAL INTERRUPT**

The Cursor Position and Vertical Interrupt signal are available when Composite Sync and Blank signals are selected

and Bit 2 of the Status Register is set to the value of 1. The Cursor Position generates a single pulse of n clocks wide during every line that the cursor is specified. The signals are generated by logically ORing (ANDing) the active LOW (HIGH) signals specified by the registers used for generating Horizontal and Vertical Gating signals. The Vertical Interrupt signal generates a pulse during the vertical interval specified. The Vertical Interrupt signal will change in the same manner as that specified for the Vertical Blanking signal.

 $\label{eq:horizontal Cursor Width = [REG(16) - REG(15)] $\times$ ckper Vertical Cursor Width = [REG(18) - REG(17)] $\times$ hper Vertical Interrupt Width = [REG(14) - REG(13)] $\times$ hper $\times$ for the property of the p$ 

## **Addressing Logic**

The register addressing logic is composed of two blocks of logic. The first is the address register and counter (ADDRCNTR), and the second is the address decode (ADDRDEC).

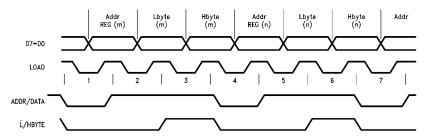
#### ADDRCNTR LOGIC

Addresses for the data registers can be generated by one of two methods. Manual addressing requires that each byte of each register that needs to be loaded needs to be addressed. To load both bytes of all 19 registers would require a total of 57 load cycles (19 address and 38 data cycles). Auto Addressing requires that only the initial register value be specified. The Auto Load sequence would require only 39 load cycles to completely program all registers (1 address and 38 data cycles). In the auto load sequence the low order byte of the data register will be written first followed by the high order byte on the next load cycle. At the

time the High Byte is written the address counter is incremented by 1. The counter has been implemented to loop on the initial value loaded into the address register. For example: If a value of 0 was written into the address register then the counter would count from 0 to 18 before resetting back to 0. If a value of 15 was written into the address register then the counter would count from 15 to 18 before looping back to 15. If a value greater than or equal to 18 is placed into the address register the counter will continuously loop on this value. Auto addressing is initiated on the falling edge of LOAD when ADDRDATA is 0 and LHBYTE is 1. Incrementing and loading of data registers will not commence until the falling edge of LOAD after ADDRDATA goes to 1. The next rising edge of LOAD will load the first byte of data. Auto Incrementing is disabled on the falling edge of LOAD after ADDRDATA and LHBYTE goes low.

#### **Manual Addressing Mode**

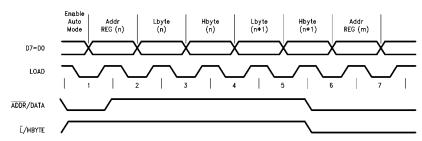
Cycle #	Load Falling Edge	Load Rising Edge		
1	Enable Manual Addressing	Load Address m		
2	Enable Lbyte Data Load	Load Lbyte m		
3	Enable Hbyte Data Load	Load Hbyte m		
4	Enable Manual Addressing	Load Address n		
5	Enable Lbyte Data Load	Load Lbyte n		
6	Enable Hbyte Data Load	Load Hbyte n		



TL/F/10137-7

## Auto Addressing Mode

Cycle #	Load Falling Edge	Load Rising Edge			
1	Enable Auto Addressing	Load Start Address n			
2	Enable Lbyte Data Load	Load Lbyte (n)			
3	Enable Hbyte Data Load	Load Hbyte (n); Inc Counter			
4	Enable Lbyte Data Load	Load Lbyte (n+1)			
5	Enable Hbyte Data Load	Load Hbyte (n + 1); Inc Counter			
6	Enable Manual Addressing	Load Address			



TL/F/10137-8

## Addressing Logic (Continued)

#### ADDRDEC LOGIC

The ADDRDEC logic decodes the current address and generates the enable signal for the appropriate register. The enable values for the registers and counters change on the falling edge of LOAD. Two types of ADDRDEC logic is enabled by 2 pair of addresses, Addresses 22 or 54 (Vectored Restart logic) and Addresses 23 or 55 (Vectored Clear logic). Loading these addresses will enable the appropriate logic and put the part into either a Restart (all counter registers are reinitialized with preprogrammed data) or Clear (all registers are cleared to zero) state. Reloading the same ADDRDEC address will not cause any change in the state of the part. The outputs during these states are frozen and the internal CLOCK is disabled. Clocking the part during a Vectored Restart or Vectored Clear state will have no effect on the part. To resume operation in the new state, or disable the Vectored Restart or Vectored Clear state, another non-ADDRDEC address must be loaded. Operation will begin in the new state on the rising edge of the non-ADDRDEC load pulse. It is recommended that an unused address be loaded following an ADDRDEC operation to prevent data registers from accidentally being corrupted. The following Addresses are used by the device.

Address 0 Status Register REG0

Address 1-18 Data Registers REG1-REG18

Address 19-21 Unused

Address 22/54 Restart Vector (Restarts Device)

Address 23/55 Clear Vector (Zeros All Registers)

Address 24-31 Unused

Address 32-50 Register Scan Addresses

Address 51-53 Counter Scan Addresses

Address 56-63 Unused

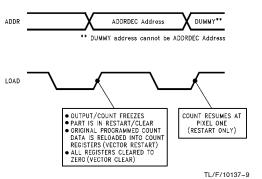
At any given time only one register at most is selected. It is possible to have no registers selected.

## **VECTORED RESTART ADDRESS**

The function of addresses 22 (16H) or 54 (36H) are similar to that of the CLR pin except that the preprogramming of the registers is not affected. It is recommended but not required that this address is read after the initial device configuration load sequence. A 1 on the ADDRDATA pin (Auto Addressing Mode) will not cause this address to automatically increment. The address will loop back onto itself regardless of the state of ADDRDATA unless the address on the Data inputs has been changed with ADDRDATA at 0.

## **VECTORED CLEAR ADDRESS**

Addresses 23 (17H) or 55 (37H) is used to clear all registers to zero simultaneously. This function may be desirable to use prior to loading new data into the Data or Status Registers. This address is read into the device in a similar fashion as all of the other registers. A 1 on the ADDRDATA pin (Auto Addressing Mode) will not cause this address to automatically increment. The address will loop back onto itself regardless of the state of ADDRDATA unless the address on the Data inputs has been changed with ADDRDATA at 0.



**FIGURE 3. ADDRDEC Timing** 

#### **GEN LOCKING**

The 'ACT715/LM1882 and 'ACT715-R/LM1882-R is designed for master SYNC and BLANK signal generation. However, the devices can be synchronized (slaved) to an external timing signal in a limited sense. Using Vectored Restart, the user can reset the counting sequence to a given location, the beginning, at a given time, the rising edge of the LOAD that removes Vector Restart. At this time the next CLOCK pulse will be CLOCK 1 and the count will restart at the beginning of the first odd line.

Preconditioning the part during normal operation, before the desired synchronizing pulse, is necessary. However, since LOAD and CLOCK are asynchronous and independent, this is possible without interruption or data and performance corruption. If the defaulted 14.31818 MHz RS-170 values are being used, preconditioning and restarting can be minimized by using the CLEAR pulse instead of the Vectored Restart operation. The 'ACT715-R/LM1882-R is better suited for this application because it eliminates the need to program a 1 into Bit 10 of the Status Register to enable the CLOCK. Gen Locking to another count location other than the very beginning or separate horizontal/vertical resetting is not possible with the 'ACT715/LM1882 nor the 'ACT715-R/LM1882-R.

#### SCAN MODE LOGIC

A scan mode is available in the ACT715/LM1882 that allows the user to non-destructively verify the contents of the registers. Scan mode is invoked through reading a scan address into the address register. The scan address of a given register is defined by the Data register address + 32. The internal Clocking signal is disabled when a scan address is read. Disabling the clock freezes the device in it's present state. Data can then be serially scanned out of the data registers through the ODD/EVEN Pin. The LSB will be scanned out first. Since each register is 12 bits wide, completely scanning out data of the addressed register will require 12 CLOCK pulses. More than 12 CLOCK pulses on the same register will only cause the MSB to repeat on the output. Re-scanning the same register will require that register to be reloaded. The value of the two horizontal counters and 1 vertical counter can also be scanned out by using address numbers 51-53. Note that before the part will scan out the data, the LOAD signal must be brought back HIGH.

## Addressing Logic (Continued)

Normal device operation can be resumed by loading in a non-scan address. As the scanning of the registers is a non-destructive scan, the device will resume correct operation from the point at which it was halted.

## **RS170 Default Register Values**

The tables below show the values programmed for the RS170 Format (using a 14.31818 MHz clock signal) and how they compare against the actual EIA RS170 Specifications. The default signals that will be output are CSYNC, CBLANK, HDRIVE and VDRIVE. The device initially starts at the beginning of the odd field of interlace. All signals have active low pulses and the clock is disabled at power up. Registers 13 and 14 are not involved in the actual signal information. If the Vertical Interrupt was selected so that a pulse indicating the active lines would be output.

Reg	D Value H		Register Description
REG0	0	000	Status Register (715/LM1882)
REG0	1024	400	Status Register (715-R/LM1882-R)
REG1	23	017	HFP End Time
REG2	91	05B	HSYNC Pulse End Time
REG3	157	09D	HBLANK Pulse End Time
REG4	910	38E	Total Horizontal Clocks
REG5	7	007	VFP End Time
REG6	13	00D	VSYNC Pulse End Time
REG7	41	029	VBLANK Pulse End Time
REG8	525	20D	Total Vertical Lines
REG9	57	039	Equalization Pulse End Time
REG10	410	19A	Serration Pulse Start Time
REG11	1	001	Pulse Interval Start Time
REG12	19	013	Pulse Interval End Time
REG13	41	029	Vertical Interrupt Activate Time
REG14	526	20E	Vertical Interrupt Deactivate Time
REG15	911	38F	Horizontal Drive Start Time
REG16	92	05C	Horizontal Drive End Time
REG17	1	001	Vertical Drive Start Time
REG18	21	015	Vertical Drive End Time

	Rate	Period
Input Clock	14.31818 MHz	69.841 ns
Line Rate	15.73426 kHz	63.556 μs
Field Rate	59.94 Hz	16.683 ms
Frame Rate	29.97 Hz	33.367 ms

## RS170 Horizontal Data

Signal	Width	μ <b>s</b>	%Н	Specification (μs)
HFP	22 Clocks	1.536		1.5 ±0.1
HSYNC Width	68 Clocks	4.749	7.47	4.7 ±0.1
HBLANK Width	156 Clocks	10.895	17.15	10.9 ±0.2
HDRIVE Width	91 Clocks	6.356	10.00	0.1H ±0.005H
HEQP Width	34 Clocks	2.375	3.74	2.3 ±0.1
HSERR Width	68 Clocks	4.749	7.47	4.7 ±0.1
HPER iod	910 Clocks	63.556	100	
		RS170 Vertical Data		
VFP	3 Lines	190.67		6 EQP Pulses
VSYNC Width	3 Lines	190.67		6 Serration Pulses
VBLANK Width	20 Lines	1271.12	7.62	0.075V ± 0.005V
VDRIVE Width	11.0 Lines	699.12	4.20	0.04V ± 0.006V
VEQP IntrvI	9 Lines		3.63	9 Lines/Field
VPERiod (field)	262.5 Lines	16.683 ms		16.683 ms/Field
VPERiod (frame)	525 Lines	33.367 ms		33.367 ms/Frame

## **Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V $_{\rm CC}$ ) -0.5V to +7.0V DC Input Diode Current (I $_{\rm IK}$ )

 $\begin{array}{cccc} V_{I} = -0.5V & -20 \text{ mA} \\ V_{I} = V_{CC} + 0.5V & +20 \text{ mA} \\ \text{DC Input Voltage (V_{I})} & -0.5V \text{ to V}_{CC} + 0.5V \end{array}$ 

DC Output Diode Current (I<sub>OK</sub>)

 $\begin{array}{c} \text{V}_{\text{O}} = -0.5\text{V} & -20\text{ mA} \\ \text{V}_{\text{O}} = \text{V}_{\text{CC}} + 0.5\text{V} & +20\text{ mA} \\ \text{DC Output Voltage (V}_{\text{O}}) & -0.5\text{V to V}_{\text{CC}} + 0.5\text{V} \end{array}$ 

DC Output Source

or Sink Current (I<sub>O</sub>)  $\pm$  15 mA

DC V<sub>CC</sub> or Ground Current

per Output Pin (I<sub>CC</sub> or I<sub>GND</sub>) ±20 mA

Storage Temperature (T<sub>STG</sub>)  $-65^{\circ}\text{C to} + 150^{\circ}\text{C}$ 

Junction Temperature (T<sub>J</sub>)

Ceramic 175°C Plastic 140°C

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature and output/input loading variables. National does not recommend operation of FACTTM circuits outside databook specifications.

# Recommended Operating Conditions

 $\begin{array}{lll} \text{Supply Voltage (V}_{CC}) & 4.5 \text{V to } 5.5 \text{V} \\ \text{Input Voltage (V}_{I}) & 0 \text{V to V}_{CC} \\ \text{Output Voltage (V}_{O}) & 0 \text{V to V}_{CC} \\ \end{array}$ 

Operating Temperature (T<sub>A</sub>)

74ACT -40°C to +85°C 54ACT -55°C to +125°C

Minimum Input Edge Rate ( $\Delta V/\Delta t$ )  $V_{IN}$  from 0.8V to 2.0V

V<sub>CC</sub> @ 4.5V, 5.5V 125 mV/ns

# DC Characteristics For 'ACT Family Devices over Operating Temperature Range (unless otherwise specified)

			ACT/LM1882		54ACT/LM1882	74ACT/LM1882			
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		$T_{A} = -55^{\circ}C$ $to + 125^{\circ}C$ $C_{L} = 50 \text{ pF}$	T <sub>A</sub> = -40°C to +85°C	Units	Conditions	
			Тур		Guaranteed L	imits			
V <sub>OH</sub>	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	4.4 5.4	V	$I_{OUT} = -50 \mu\text{A}$	
		4.5 5.5		3.86 4.86	3.7 4.7	3.76 4.76	V V	$V_{IN} = V_{IL}/V_{IH}$ $V_{OH} = -8 \text{ mA}$	
V <sub>OL</sub>	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	0.1 0.1	V V	$I_{OUT} = 50 \mu A$	
		4.5 5.5		0.36 0.36	0.5 0.5	0.44 0.44	V V	$V_{IN} = V_{IL}/V_{IH}$ $V_{OH} = +8 \text{ mA}$	
l <sub>OLD</sub>	Minimum Dynamic Output Current	5.5			32.0	32.0	mA	V <sub>OLD</sub> = 1.65V	
I <sub>OHD</sub>	Minimum Dynamic Output Current	5.5			-32.0	-32.0	mA	V <sub>OHD</sub> = 3.85V	
I <sub>IN</sub>	Maximum Input Leakage Current	5.5		±0.1	± 1.0	± 1.0	μΑ	$V_{I} = V_{CC}$ , GND	
Icc	Supply Current Quiescent	5.5		8.0	160	80	μΑ	$V_{IN} = V_{CC}$ , GND	
ICCT	Maximum I <sub>CC</sub> /Input	5.5	0.6		1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1V$	

<sup>\*</sup>All outputs loaded; thresholds on input associated with input under test.

Note 1: Test Load 50 pF,  $500\Omega$  to Ground.

# **AC Electrical Characteristics**

Symbol Parameter		V <sub>CC</sub> (V)	ACT/LM1882 $T_{A} = +25^{\circ}C$ $C_{L} = 50 \text{ pF}$		54ACT/LM1882  T <sub>A</sub> = -55°C  to +125°C  C <sub>L</sub> = 50 pF		74ACT/LM1882  T <sub>A</sub> = -40°C  to +85°C  C <sub>I</sub> = 50 pF		Units	
			Min	Тур	Max	Min	Max	Min	Max	1
f <sub>MAXI</sub>	Interlaced f <sub>MAX</sub> (HMAX/2 is ODD)	5.0	170	190		130		150		MHz
f <sub>MAX</sub>	Non-Interlaced f <sub>MAX</sub> (HMAX/2 is EVEN)	5.0	190	220		145		175		MHz
t <sub>PLH1</sub>	Clock to Any Output	5.0	4.0	13.0	15.5	3.5	19.5	3.5	18.5	ns
t <sub>PLH2</sub>	Clock to ODDEVEN (Scan Mode)	5.0	4.5	15.0	17.0	3.5	22.0	3.5	20.5	ns
t <sub>PLH3</sub>	Load to Outputs	5.0	4.0	11.5	16.0	3.0	20.0	3.0	19.5	ns

# **AC Operating Requirements**

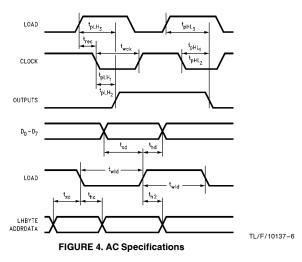
	Parameter		ACT/I	M1882	54ACT/LM1882	74ACT/LM1882		
Symbol		V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C		$T_A = -55^{\circ}C$ to $+125^{\circ}C$	$T_{A} = -40^{\circ}C$ to $+85^{\circ}C$	Units	
			Тур		Guaranteed Mini	Guaranteed Minimums		
t <sub>sc</sub>	Control Setup Time ADDR/DATA to LOAD — L/HBYTE to LOAD —	5.0	3.0 3.0	4.0 4.0	4.5 4.5	4.5 4.5	ns ns	
t <sub>sd</sub>	Data Setup Time D7-D0 to LOAD+	5.0	2.0	4.0	4.5	4.5	ns	
t <sub>hc</sub>	Control Hold Time LOAD – to ADDR/DATA LOAD – to L/HBYTE	5.0	0	1.0 1.0	1.0 1.0	1.0 1.0	ns ns	
t <sub>hd</sub>	Data Hold Time LOAD+ to D7-D0	5.0	1.0	2.0	2.0	2.0	ns	
t <sub>rec</sub>	LOAD+ to CLK (Note 1)	5.0	5.5	7.0	8.0	8.0	ns	
t <sub>wld</sub> –	Load Pulse Width LOW HIGH	5.0 5.0	3.0 3.0	5.5 5.0	5.5 7.5	5.5 7.5	ns ns	
t <sub>wclr</sub>	CLR Pulse Width HIGH	5.0	5.5	6.5	9.5	9.5	ns	
t <sub>wck</sub>	CLOCK Pulse Width (HIGH or LOW)	5.0	2.5	3.0	4.0	3.5	ns	

Note 1: Removal of Vectored Reset or Restart to Clock.

# Capacitance

Symbol	Parameter	Тур	Units	Conditions
C <sub>IN</sub>	Input Capacitance	7.0	pF	$V_{CC} = 5.0V$
C <sub>PD</sub>	Power Dissipation Capacitance	17.0	pF	$V_{CC} = 5.0V$

#### **AC Operating Requirements** (Continued)



# Additional Applications Information POWERING UP

The 'ACT715/LM1882 default value for Bit 10 of the Status Register is 0. This means that when the CLEAR pulse is applied and the registers are initialized by loading the default values the CLOCK is disabled. Before operation can begin, Bit 10 must be changed to a 1 to enable CLOCK. If the default values are needed (no other programming is required) then Figure 5 illustrates a hardwired solution to facilitate the enabling of the CLOCK after power-up. Should control signals be difficult to obtain, Figure 6 illustrates a possible solution to automatically enable the CLOCK upon power-up. Use of the 'ACT715-R/LM1882-R eliminates the need for most of this circuitry. Modifications of the Figure 6 circuit can be made to obtain the lone CLEAR pulse still needed upon power-up.

Note that, although during a Vectored Restart none of the preprogrammed registers are affected, some signals are affected for the duration of one frame only. These signals are the Horizontal and Vertical Drive signals. After a Vectored Restart the beginning of these signals will occur at the first CLK. The end of the signals will occur as programmed. At the completion of the first frame, the signals will resume to their programmed start and end time.

#### PREPROGRAMMING "ON-THE-FLY"

Although the 'ACT715/LM1882 and 'ACT715-R/LM1882-R are completely programmable, certain limitations must be set as to when and how the parts can be reprogrammed. Care must be taken when reprogramming any End Time registers to a new value that is lower than the current value. Should the reprogramming occur when the counters are at a count after the new value but before the old value, then the counters will continue to count up to 4096 before rolling over.

For this reason one of the following two precautions are recommended when reprogramming "on-the-fly". The first recommendation is to reprogram horizontal values during the horizontal blank interval only and/or vertical values during the vertical blank interval only. Since this would require delicate timing requirements the second recommendation may be more appropriate.

The second recommendation is to program a Vectored Restart as the final step of reprogramming. This will ensure that all registers are set to the newly programmed values and that all counters restart at the first CLK position. This will avoid overrunning the counter end times and will maintain the video integrity.

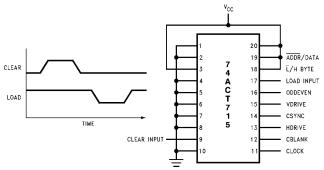
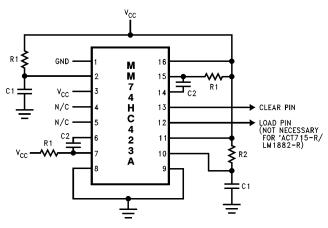


FIGURE 5. Default RS170 Hardwire Configuration

TL/F/10137-10

#### **Additional Applications Information (Continued)**



Note: A 74HC221A may be substituted for the 74HC423A Pin 6 and Pin 14 must be hardwired to GND

Components

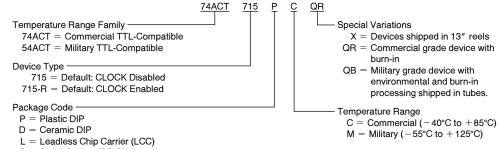
R1: 4.7k C1: 10 µF R2: 10k C2: 50 pF

FIGURE 6. Circuit for Clear and Load Pulse Generation

TL/F/10137-11

#### **Ordering Information**

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



S = Small Outline (SOIC)

LM1882CM = Commercial Small Outline (SOIC) Default: LM1882CN = Commercial Plastic DIP **CLOCK** LM1882J/883 = Military Ceramic Dip

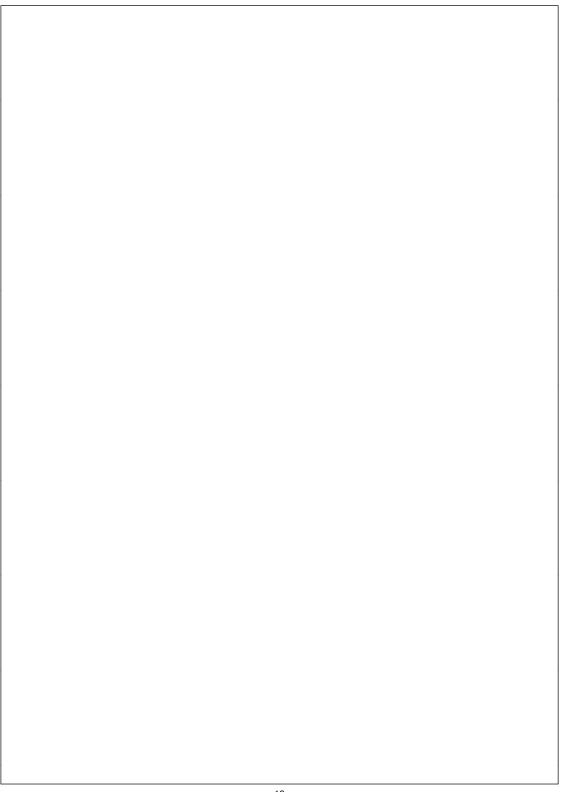
OR

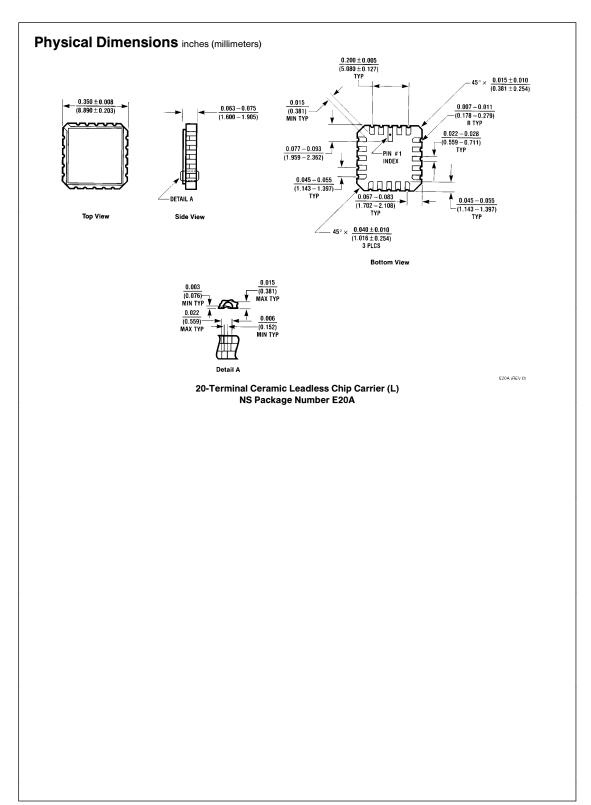
Disabled LM1882E/883 = Military Leadless Chip Carrier

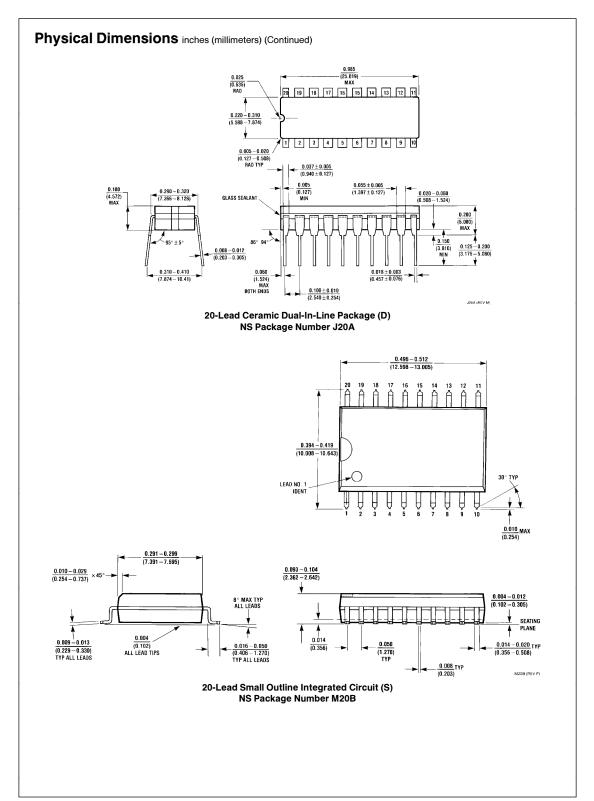
LM1882-RCM = Commercial Small Outline (SOIC) Default

CLOCK LM1882-RCN = Commercial Plastic DIP LM1882-RJ/883 = Military Ceramic Dip Enabled

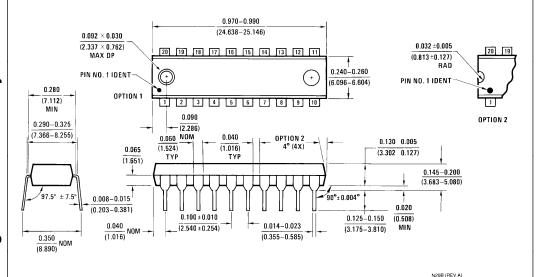
LM1882-RE/883 = Military Leadless Chip Carrier







#### Physical Dimensions inches (millimeters) (Continued)



20-Lead Plastic Dual-In-Line Package (P) NS Package Number N20B

#### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation 1111 West Bardin Road Arlington, TX 76017 Tel: 1(800) 272-9959 Fax: 1(800) 737-7018 National Semiconductor Europe

Fax: (+49) 0-180-530 85 86 Email: cnjwge@tevm2.nsc.com Deutsch Tel: (+49) 0-180-530 85 85 English Tel: (+49) 0-180-532 78 32 Français Tel: (+49) 0-180-532 93 58 Italiano Tel: (+49) 0-180-534 16 80 National Semiconductor Hong Kong Ltd. 13th Floor, Straight Block, Ocean Centre, 5 Canton Rd.

Tsimshatsui, Kowloon Hong Kong Tel: (852) 2737-1600 Fax: (852) 2736-9960 National Semiconductor Japan Ltd. Tel: 81-043-299-2309 Fax: 81-043-299-2408

#### **QUAD OPERATIONAL AMPLIFIERS**

**14 DIP** 

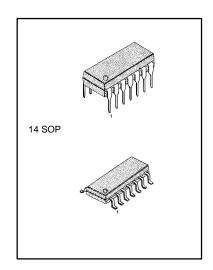
The LM224 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide voltage range.

Operation from split power supplies is also possible so long as the difference between the two supplies is 3 volts to 32 volts.

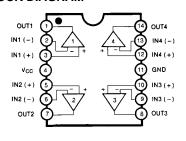
Application areas include transducer amplifier, DC gain blocks and all the conventional OP amp circuits which now can be easily implemented in single power supply systems.

#### **FEATURES**

- Internally frequency compensated for unity gain
- Large DC voltage gain: 100dB
- Wide power supply range: LM224/A, LM324/A: 3V ~32V (or ±1.5 ~ 15V)
   LM2902: 3V~26V (or ±1.5V ~ 13V)
- Input common-mode voltage range includes ground
- $\bullet~$  Large output voltage swing: 0V DC to  $V_{\text{CC}}\text{-}1.5V~\text{DC}$
- · Power drain suitable for battery operation.



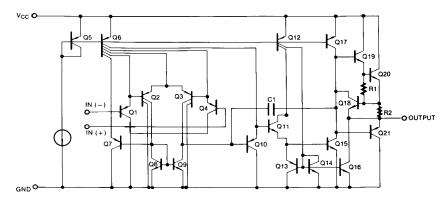
#### **BLOCK DIAGRAM**



#### **ORDERING INFORMATION**

Device	Package	Operating Temperature
LM324N	14 DIP	
LM324AN	14 DIF	0 . 7000
LM324M	14 SOP	0 ~ + 70°C
LM324AM	14 301	
LM224N	14 DIP	
LM224AN	14 DIF	-25 ~ +85 °C
LM224M	14 SOP	-25 ~ +05 C
LM224AM	14 301	
LM2902N	14 DIP	-40 ~ + 85 °C
LM2902M	14 SOP	-40 ~ + 85 °C

#### SCHEMATIC DIAGRAM (One Section Only)





# LM224/A, LM324/A, LM2902

## **QUAD OPERATIONAL AMPLIFIER**

#### **ABSOLUTE MAXIMUM RATINGS**

Characteristic	Symbol	LM224/LM224A	LM324/LM324A	LM2902	Unit
Power Supply Voltage	V <sub>cc</sub>	±18 or 32	±18 or 32	±13 or 26	V
Differential Input Voltage	$V_{I(DIFF)}$	32	32	26	V
Input Voltage	VI	-0.3 to + 32	-0.3 to +32	-0.3 to +26	V
Output Short Circuit to GND					
V <sub>CC</sub> ≤15V T <sub>A</sub> =25 °C(One Amp)		Continuous	Continuous	Continuous	
Power Dissipation	$P_D$	570	570	570	mW
Operating Temperature Range	T <sub>OPR</sub>	-25 ~ +85	0 ~ + 70	-40 ~ + 85	°C
Storage Temperature Range	$T_{STG}$	-65 ~ <b>+</b> 150	-65 ~ <b>+</b> 150	-65 ~ + 150	°C

#### **ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub>=5.0V, V<sub>EE</sub>=GND, T<sub>A</sub>=25  $^{\circ}$ C, unless otherwise specified)

	0			ı	M22	4	L	M32	4	LM2902			
Characteristic	Symbol	Test Condition	Test Conditions		Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Input Offset Voltage	V <sub>IO</sub>	$V_{CM} = 0V \text{ to } V_{CC} = 1.5$ $V_{O(P)} = 1.4V, R_S = 0\Omega$	V		1.5	5.0		1.5	7.0		1.5	7.0	mV
Input Offset Current	I <sub>IO</sub>				2.0	30		3.0	50		3.0	50	nA
Input Bias Current	I <sub>BIAS</sub>				40	150		40	250		40	250	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	$V_{CC} = 30V$ ( $V_{CC} = 26V$ for KA290	2)	0		V <sub>CC</sub> -1.5	0	V <sub>CC</sub> -1.5		0		V <sub>CC</sub> -1.5	٧
		$R_L = \infty, V_{CC} = 30V$ (all	Amps)		1.0	3		1.0	3		1.0	3	mA
Supply Current	Icc	$R_L = \infty, V_{CC} = 5V \text{ (all Amps)}$ $(V_{CC} = 26V \text{ for KA2902})$			0.7	1.2		0.7	1.2		0.7	1.2	mA
Large Signal Voltage Gain	G <sub>V</sub>	$V_{CC} = 15V, R_L \ge 2K\Omega$ $V_{O(P)} = 1V \text{ to } 11V$		50	100		25	100			100		V/mV
	.,	$V_{CC} = 30V$	$R_L = 2K\Omega$	26			26			22			V
Output Voltage Swing	V <sub>O(H)</sub>	V <sub>CC</sub> =26V for 2902	$R_L = 10K\Omega$	27	28		27	28		23	24		V
	V <sub>O(L)</sub>	$V_{CC} = 5V, R_L \ge 10K\Omega$			5	20		5	20		5	100	mV
Common-Mode Rejection Ratio	CMRR			70	85		65	75		50	75		dB
Power Supply Rejection Ratio	PSRR			65	100		65	100		50	100		dB
Channel Separation	CS	f = 1KHz to 20KHz			120			120			120		dB
Short Circuit to GND	I <sub>SC</sub>				40	60		40	60		40	60	mA
	I <sub>SOURCE</sub>	$V_{I(+)} = 1V, V_{I(-)} = 0V$ $V_{CC} = 15V, V_{O(P)} = 2V$		20	40		20	40		20	40		mA
Output Current		$V_{I(+)} = 0V, V_{I(-)} = 1V$ $V_{CC} = 15V, V_{O(P)} = 2V$	$V_{I(+)} = 0V, \ V_{I(-)} = 1V$		13		10	13		10	13		mA
	I <sub>SINK</sub>	$V_{I(+)} = 0V, V_{I(-)} = 1V$ $V_{CC} = 15V, V_{O(R)} = 200mV$		12	45		12	45					μΑ
Differential Input Voltage	V <sub>I(DIFF)</sub>					V <sub>cc</sub>			V <sub>cc</sub>			V <sub>CC</sub>	٧



#### **ELECTRICAL CHARACTERISTICS**

 $(V_{CC} = 5.0V, V_{EE} = GND, unless otherwise specified)$ 

The following specification apply over the range of -25 °C  $\leq$  T<sub>A</sub>  $\leq$  + 85 °C for the LM224; and the 0 °C  $\leq$  T<sub>A</sub>  $\leq$  +70 °C for the LM324; and the - 40 °C  $\leq$  T<sub>A</sub>  $\leq$  +85 °C for the LM2902

Characteristic	Symbol	Test Conc	litiono	I	_M22	4	ı	M32	4	LM2902			Unit
Characteristic	Syllibol	rest Conc	rest Conditions		Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Input Offset Voltage	V <sub>IO</sub>	$V_{ICM} = 0V \text{ to } V_{CC} = V_{O(P)} = 1.4V, R_S = 0$				7.0			9.0			10.0	mV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$				7.0			7.0			7.0		μV/°C
Input Offset Current	I <sub>IO</sub>					100			150			200	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$				10			10			10		pA/°C
Input Bias Current	I <sub>BIAS</sub>					300			500			500	nA
Input Common-Mode Voltage Range	$V_{IC(R)}$	$V_{CC} = 30V$ $(V_{CC} = 26V \text{ for KA2})$	902)	0		V <sub>CC</sub> -2.0	0		V <sub>CC</sub> -2.0	0		V <sub>CC</sub> -2.0	V
Large Signal Voltage Gain	Gv	$V_{CC} = 15V, R_L \ge 2.0$ $V_{O(P)} = 1V \text{ to } 11V$	ΚΩ	25			15			15			V/mV
	.,	$V_{CC} = 30V$	$R_L = 2K\Omega$	26			26			22			V
Output Voltage Swing	$V_{O(H)}$	V <sub>CC</sub> =26V for 2902	$R_L = 10K\Omega$	27	28		27	28		23	24		V
	$V_{O(L)}$	V <sub>CC</sub> = 5V, R <sub>L</sub> ≥10KΩ	2		5	20		5	20		5	100	mV
	I <sub>SOURCE</sub>	$V_{I(+)} = 1V, V_{I(-)} = 0V$ $V_{CC} = 15V, V_{O(P)} = 2$	2V	10	20		10	20		10	20		mA
Output Current	I <sub>SINK</sub>	$V_{I(+)} = 0V, V_{I(-)} = 1V$ $V_{CC} = 15V, V_{O(P)} = 1$		10	13		5	8		5	8		mA
Differential Input Voltage	$V_{I(DIFS)}$					V <sub>cc</sub>			V <sub>cc</sub>			V <sub>cc</sub>	V



# **QUAD OPERATIONAL AMPLIFIER**

#### **ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub>=50V, V<sub>EE</sub> = GND,  $T_A$ =25 °C, unless otherwise specified)

Characteristic	Cumhal	Test Conditions		L	M224	Α	LM324A			Unit	
Characteristic	Symbol	l est Condit	tions	Min	Тур	Max	Min	Тур	Max	Oill	
Input Offset Voltage	V <sub>IO</sub>	$V_{CM} = 0V \text{ to } V_{CC} = 1.$ $V_{O(P)} = 1.4V, R_S = 0$	$V_{CM} = 0V \text{ to } V_{CC} = 1.5V$ $V_{CM} = 1.4V \text{ Rs} = 0.0$		1.0	3.0		1.5	3.0	mV	
Input Offset Current	I <sub>IO</sub>				2	15		3.0	30	nA	
Input Bias Current	I <sub>BIAS</sub>				40	80		40	100	nA	
Input Common-Mode Voltage Range	V <sub>I(R)</sub>	V <sub>CC</sub> = 30V		0		V <sub>CC</sub> -1.5	0		V <sub>CC</sub> -1.5	V	
Supply Current (All Amps)	Icc	$V_{CC} = 30V$			1.5	3		1.5	3	mΑ	
Supply Current (All Amps)	ICC	$V_{CC} = 5V$			0.7	1.2		0.7	1.2	mΑ	
Large Signal Voltage Gain	Gv	$V_{CC} = 15V, R_L \ge 2 K\Omega$ $V_{O(P)} = 1V \text{ to } 11V$	Ω	50	100		25	100		V/mV	
		V <sub>CC</sub> = 30V	$R_L = 2 K\Omega$	26			26			V	
Output Voltage Swing	$V_{O(H)}$	$V_{CC} = 26V \text{ for } 2902$	$R_L = 10 \text{ K}\Omega$	27	28		27	28		V	
	V <sub>O(L)</sub>	$V_{CC} = 5V, R_1 \ge 10 \text{ K}\Omega$	2		5	20		5	20	mV	
Common-Mode Rejection Ratio	CMRR			70	85		65	85		dB	
Power Supply Rejection Ratio	PSRR			65	100		65	100		dB	
Channel Separation	CS	f = 1KHz to 20KHz			120			120		dB	
Short Circuit to GND	I <sub>sc</sub>				40	60		40	60	mA	
	I <sub>SOURCE</sub>	$V_{I(+)} = 1V, V_{I(-)} = 0V$ $V_{CC} = 15V$		20	40		20	40		mA	
Output Current		$V_{I(+)} = 0V, V_{I(-)} = 1V$ $V_{CC} = 15V, V_{O(P)} = 2V$	V	10	20		10	20		mA	
	I <sub>SINK</sub>	$V_{I(+)} = 0v, V_{I(-)} = 1V$ $V_{CC} = 15V, V_{O(P)} = 20$		12	50		12	50		μΑ	
Differential Input Voltage	$V_{I(DIFF)}$					$V_{CC}$			$V_{CC}$	V	



## **QUAD OPERATIONAL AMPLIFIER**

#### **ELECTRICAL CHARACTERISTICS**

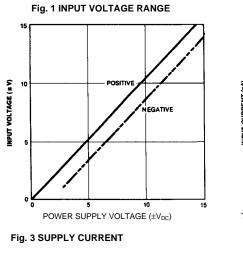
( $V_{CC}$  = 5.0V,  $V_{EE}$  = GND, unless otherwise specified) The following specification apply over the range of -25°C  $\leq$  T<sub>A</sub>  $\leq$  + 85 °C for the LM224A; and the 0 °C  $\leq$  T<sub>A</sub>  $\leq$ +70 °C for the LM324A

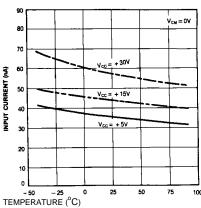
Characteristic		Test Conditions		L	M224	Ą	L	M324	A	l lmi4	
Characteristic	Symbol	lest Con	rest conditions		Тур	Max	Min	Тур	Max	Unit	
Input Offset Voltage	V <sub>IO</sub>	$V_{CM} = 0V \text{ to } V$ $V_{O(P)} = 1.4V, F$				4.0			5.0	mV	
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$				7.0	20		7.0	30	μV/°C	
Input Offset Current	I <sub>IO</sub>					30			75	nA	
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$				10	200		10	300	pA/°C	
Input Bias Current	I <sub>BIAS</sub>				40	100		40	200	nA	
Input Common-Mode Voltage Range	V <sub>I(R)</sub>	V <sub>CC</sub> = 30V		0		V <sub>CC</sub> -2.0	0		V <sub>CC</sub> -2.0	V	
Large Signal Voltage Gain	G∨	$V_{CC} = 15V, R_L$	≥ 2.0KΩ	25			15			V/mV	
		V <sub>CC</sub> = 30V	$R_L = 2K\Omega$	26			26				
Output Voltage Swing	$V_{O(P-P)}$	VCC = 00 V	$R_L = 10K\Omega$	27	28		27	28		V	
		$V_{CC} = 5V, R_L \ge$	:10ΚΩ		5	20		5	20	mA	
	I <sub>SOURCE</sub>	$V_{l(+)} = 1V, V_{l(-)} = 0V$ $V_{CC} = 15V$ $V_{l(+)} = 0V, V_{l(-)} = 1V$ $V_{CC} = 15V$		10	20		10	20		mA	
Output Current	I <sub>SINK</sub>			5	8		5	8		mA	
Differential Input Voltage	$V_{I(DIFF)}$		•			$V_{CC}$			$V_{CC}$	V	



Fig. 2 INPUT CURRENT

#### **TYPICAL PERFORMANCE CHARACTERISTICS**





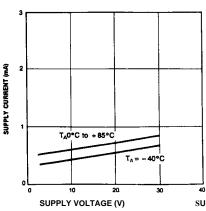


Fig. 4 VOLTAGE GAIN

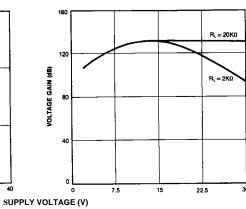


Fig. 5 OPEN LOOP FREGUENCY RESPONSE

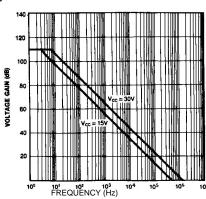
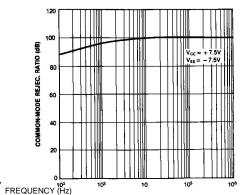
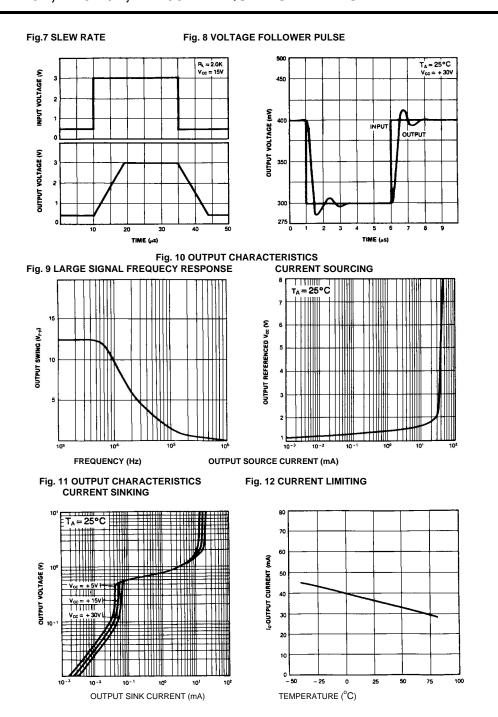


Fig. 6 COMMON.MOOE REJECTION RATIO





SEMICONDUCTOR TM





#### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

#### **PRODUCT STATUS DEFINITIONS**

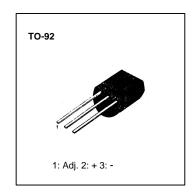
#### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

#### PROGRAMMABLE SHUNT REGULATOR

The LM336-2.5/B integrated Circuits are precision 2.5V shunt regulators. The monolithic IC voltage references operates as a low temperature coefficient 2.5V zener with 0.2 $\Omega$  dynamic impedance. A third terminal on the KA336-2.5/B allow the reference voltage and temperature coefficient to be trimmed easily.

LM3362.5/B are useful as a precision 2.5V low voltage reference for digital voltmeters, power supplies or op amp circuitry. The 2.5V make it convenient to obtain a stable reference from low voltage supplies. Further, since the LM336-2.5/B operate as shunt regulators, they can be used as either a positive or negative voltage reference.



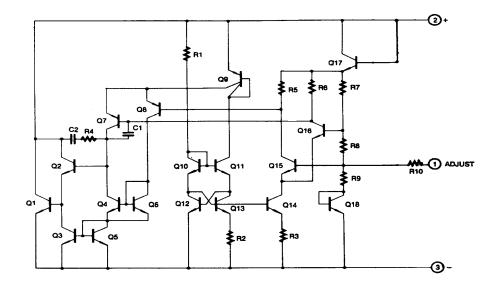
#### **FEATURES**

- Low temperature coefficient
- Guaranteed temperature stability 4mV typical
- ullet 0.2  $\Omega$  dynamic impedance
- $\bullet$  ±1.0% initial tolerance available.
- Easily trimmed for minimum temperature drift

#### **ORDERING INFORMATION**

Device	Package	Operating Temperature
LM336Z-2.5		2 7200
LM336Z-2.5B	TO-92	0 ~ +70°C
LM236Z-2.5		-25 ~ +85°C

#### **SCHEMATIC DIAGRAM**





#### LM336-2.5/B/LM236-2.5 (KA336-2.5, KA236-2.5) PROGRAMMABLE SHUNT REGULATOR

#### **ABSOLUTE MAXIMUM RATINGS**

Characteristic	Symbol	Value	Unit
Reverse Current	I <sub>R</sub>	15	mA
Forward Current	l <sub>F</sub>	10	mA
Operating Temperature Range LM336-2.5/B LM236-2.5	$T_OPR$	0 ~ + 70 - 25 ~ +85	°C °C
Storage Temperature Range	T <sub>STG</sub>	- 60 ~ <b>+</b> 150	°C

#### $\textbf{ELECTRICAL CHARACTERISTICS} \ (T_{MIN} < T_A \ < T_{MAX}, \ unless \ otherwise \ specified)$

Observatoriation	0	Tank Complisions	L	M336/23	36	L	_M336E	3	
Characteristic	Symbol	Test Conditions	Min	Тур	Max	Min	Тур	Max	
Reverse Breakdown Voltage	$V_{R}$	$T_A = +25^{\circ}C$ $I_R = 1mA$	2.44	2.49	2.54	2.465	2.49	2.515	V
Reverse Breakdown Change with Current	$\Delta V_R/\Delta I_R$	$T_A = +25^{\circ}C$ $400\mu A \le I_R \le 10mA$		2.6	6		2.6	10	mV
Reverse Dynamic Impedance	$Z_D$	$T_A = +25$ °C $I_R = 1$ mA		0.2	0.6		0.2	1	Ω
Temperature Stability	ST⊤	$I_R = 1mA$ $T_{MIN} \le T_A \le T_{MAX}$		1.8	6		1.8	6	mV
Reverse Breakdown Change with Current	$\Delta V_R/\Delta I_R$	$T_{MIN} \le T_A \le T_{MAX}$ $400\mu A \le I_R \le 10mA$		3	10		3	12	mV
Reverse Dynamic Impedance	$Z_D$	$I_R = 1mA$ $T_{MIN} \le T_A \le T_{MAX}$		0.4	1		0.4	1.4	Ω
Long Term Stability	ST	$I_{R} = 1 \text{mA}$ $T_{MIN} \le T_{A} \le T_{MAX}$		20			20		ppm

LM236:  $T_{MIN} = -25^{\circ}C$ ,  $T_{MAX} = +85^{\circ}C$ LM336:  $T_{MIN} = 0^{\circ}C$ ,  $T_{MAX} = +70^{\circ}C$ 



#### TYPICAL PERFORMANCE CHARACTERISTICS

Fig. 1. Reverse Voltage Change

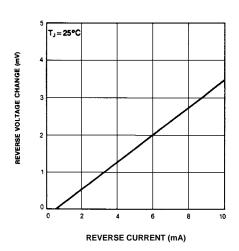


Fig. 2 Reverse Characteristics

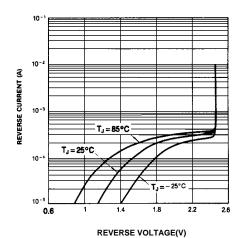


Fig. 3 Temperature Drift

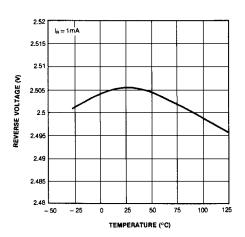
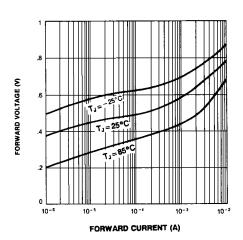


Fig. 4 Forward Characteristics



FAIRCHILD SEMICONDUCTOR TM

#### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

#### **PRODUCT STATUS DEFINITIONS**

#### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

14 DIP

14 SOP

#### **QUAD DIFFERENTIAL COMPARATOR**

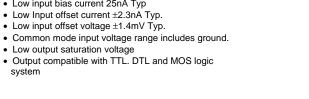
The LM239 series consists of four independent voltage comparators designed to operate from single power supply over a wide voltage range.

#### **FEATURES**

- Single or dual supply operation
- Wide range of supply voltage

LM239/A, LM339/A, LM2901: 2 ~ 36V (or ±1 ~ ±18V) LM3302: 2 ~ 28V (or ±1 ~ ±14V)

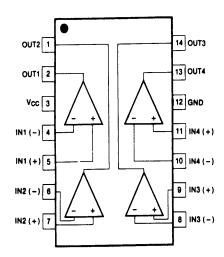
- Low supply current drain 800μA Typ
- · Open collector outputs for wired and connectors
- Low input bias current 25nA Typ



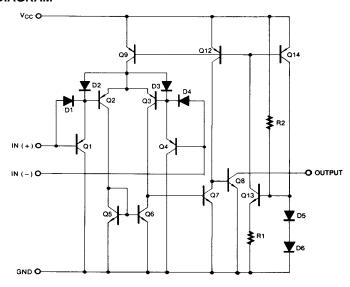
# **ORDERING INFORMATION**

Device	Package	Operating Temperature
LM339N	14 DIP	
LM339AN	14 DIP	
LM339M	14 SOP	0 ~ +70°C
LM339AM	14 30F	
LM239N	14 DIP	
LM239AN	14 DIF	-25 ~ + 85°C
LM239M	14 SOP	-25 ~ + 85°C
LM239AM	14 30F	
LM2901N	14 DIP	
LM2901M	14 SOP	-40 ~ + 85°C
LM3302N	14 DIP	-40 ~ + 65 C
LM3302M	14 SOP	

#### **BLOCK DIAGRAM**



#### **SCHEMATIC DIAGRAM**



#### **ABSOLUTE MAXIMUM RATINGS**

Characteristic	Symbol	Value	Unit
Supply Voltage	V <sub>cc</sub>	±18 or 36	V
Supply Voltage Only LM3302	V <sub>cc</sub>	±14 or 28	V
Differential Input Voltage	V <sub>I(DIFF)</sub>	36	V
Differential Input Voltage Only LM3302	$V_{I(DIFF)}$	28	V
Input Voltage	$V_{l}$	- 0.3 to +36	V
Input Voltage Only LM3302	$V_{l}$	- 0.3 to +28	V
Output Short Circuit to GND		Continuous	
Power Dissipation	$P_D$	570	mW
Operating Temperature LM339/LM339A		0 ~ + 70	°C
LM239/LM239A	T <sub>OPR</sub>	- 25 ~ + 85	°C
LM2901/LM3302		- 40 ~ + 85	°C
Storage Temperature	T <sub>STG</sub>	- 65 ~ + 150	°C



#### **ELECTRICAL CHARACTERISTICS**

 $(V_{CC} = 5V, T_A = 25^{\circ}C, unless otherwise specified)$ 

Ob ana staniatia	0	T4 O		LM2	39A/L	M339A	LN	I Imit		
Characteristic	Symbol	Test Conditions	5	Min	Тур	Max	Min	Тур	Max	Unit
l	V <sub>IO</sub>	$V_{CM} = 0V$ to $V_{CC} = 1.5V$			±1	±2		±1.4	±5	
Input Offset Voltage	VIO	$V_{O(P)} = 1.4V, R_S = 0\Omega$	NOTE 1			±4.0			±9.0	mV
l					±2.3	±50		±2.3	±50	nA
Input Offset Current	I <sub>IO</sub>		NOTE 1			±150			±150	ПА
Input Bias Current	I <sub>BIAS</sub>				57	250		57	250	nA
	IBIAS		NOTE 1			400			400	11/1
Input Common Mode	V <sub>I(R)</sub>			0		V <sub>CC</sub> -1.5	0		V <sub>CC</sub> -1.5	V
Voltage Range	I(IV)		NOTE 1	0		V <sub>CC</sub> -2	0		V <sub>CC</sub> -2	V
Supply Current	Icc		R <sub>L</sub> = ∞		1.1	2.0		1.1	2.0	mA
Voltage Gain	G∨	V <sub>CC</sub> =15V, R <sub>L</sub> ≥15KΩ(for larg	je swing)	50	200		50	200		V/mV
Large Signal Response Time	t <sub>RES</sub>	V <sub>I</sub> =TTL Logic Swing V <sub>REF</sub> =1.4V, V <sub>RL</sub> =5V, R <sub>L</sub> =5.	1KO		350			350		ns
Response Time	t <sub>RES</sub>	$V_{RL} = 5V, R_L = 5.1K\Omega$	11/22		1.4			1.4		μs
Output Sink Current	I <sub>SINK</sub>	$V_{I(-)} \ge 1V$ , $V_{I(+)} = 0V$ , $V_{O(P)} \le 1.5$	V	6	18		6	18		mΑ
Output Saturation	$V_{SAT}$	$V_{I(-)} \ge 1V, V_{I(+)} = 0V$			140	400		140	400	.,
Voltage	* SAT	I <sub>SINK</sub> =4mA	NOTE 1			700			700 mV	
Output Leakage	I <sub>O(LKG)</sub>	$V_{I(-)} = 0V$	$V_{O(P)} = 5V$		0.1			0.1		nA
Current	·O(LKG)	$V_{I(+)} = 1V$	$V_{O(P)} = 30V$			1.0			1.0	μΑ
Differential Voltage	$V_{I(DIFF)}$		NOTE 1			36			36	V

Note 1.

LM339/A:  $0 \le T_A \le +70^{\circ}C$ LM239/A:  $-25 \le T_A \le +85^{\circ}C$ LM2901/3302:  $-40 \le T_A \le +85^{\circ}C$ 



#### **ELECTRICAL CHARACTERISTICS**

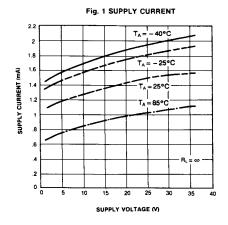
 $(V_{CC} = 5V, T_A = 25^{\circ}C, unless otherwise specified)$ 

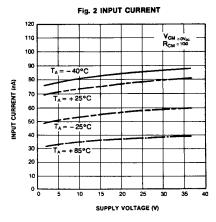
Characteristic	Symbol	Test Condit	iono		LM29	01		Unit			
Citaracteristic	Symbol	rest condit	10115	Min	Тур	Max	Min	Тур	Max	Jt	
	\/	$V_{CM} = 0V$ to $V_{CC} = 1.5V$			2	7		2	20	.,	
Input Offset Voltage	V <sub>IO</sub>	$V_{O(P)} = 1.4V, R_S = 0\Omega$	NOTE 1		თ	15			40	mV	
Input Offset Current	I <sub>IO</sub>				2.3	50		3	100	nA	
Input Onset Current	10		NOTE 1		50	200			300	шА	
Input Bias Current	I <sub>BIAS</sub>				57	250		57	250	nA	
Input bias Current	BIAS		NOTE 1		200	500			1000	ПА	
Input Common Mode	V <sub>I(R)</sub>			0		V <sub>CC</sub> -1.5	0		V <sub>CC</sub> -1.5	V	
Voltage Range	V I(R)		NOTE 1	0		V <sub>CC</sub> -2	0		V <sub>CC</sub> -2	V	
Supply Current	Icc		R <sub>L</sub> =∞		1.1	2.0		1.1	2.0	mA	
Сирріу Сипопі	•00		$R_L = \infty$ , $V_{CC} = 30V$		1.6	2.5				ША	
Voltage Gain	G <sub>V</sub>	$V_{CC}$ =15V, $R_L \ge 15K\Omega$ (for I	arge swing)	25	100		2	30		V/mV	
Large Signal Response Time	t <sub>RES</sub>	$V_I = TTL Logic Swing$ $V_{RFF} = 1.4V, V_{RI} = 5V, R_I = 5V$	-5 1KO		350			350		ns	
Response Time	t <sub>RES</sub>	$V_{RI}$ =5V, $R_{I}$ =5.1K $\Omega$	-0.1142		1.4			1.4		แร	
Output Sink Current	I <sub>SINK</sub>	$V_{I(-)} \ge 1V$ , $V_{I(+)} = 0V$ , $V_{O(P)} \le 1$	1.5V	6	18		6	18		mΑ	
Output Saturation	.,	$V_{I(-)} \ge 1V, V_{I(+)} = 0V$			140	400		140	400		
Voltage	V <sub>SAT</sub>	I <sub>SINK</sub> =4mA	NOTE 1			700			700	mV	
Output Leakage	I <sub>O(LKG)</sub>	$V_{I(-)} = 0V$	$V_{O(P)} = 5V$		0.1			0.1		nA	
Current	IO(LKG)	$V_{I(+)} = 1V$	$V_{O(P)} = 30V$			1.0			1.0	μΑ	
Differential Voltage	$V_{I(DIFF)}$		NOTE 1			36			36	V	

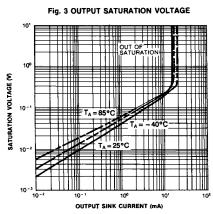
Note 1. LM339/A:  $0 \le T_A \le +70^{\circ}C$ LM239/A: -25≤T<sub>A</sub>≤ +85°C LM2901/3302: -40≤T<sub>A</sub>≤ +85°C

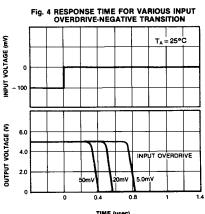


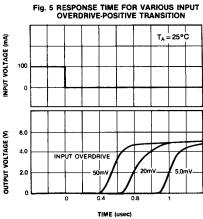
#### **TYPICAL PERFORMANCE CHARACTERISTICS**











INPUT VOLTAGE (mA) OUTPUT VOLTAGE (V)

FAIRCHILD SEMICONDUCTOR TM

#### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

#### **PRODUCT STATUS DEFINITIONS**

#### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

14 DIP

#### **QUAD OPERATIONAL AMPLIFIERS**

The LM248/LM348 is a true quad LM741. It consists of four independent, high-gain, internally compensated, low-power operational amplifiers which have been designed to provide functional characteristics identical to those of the familiar LM741 operational amplifier. In addition the total supply current for all four amplifiers is comparable to the Supply current of a single LM741 type OP Amp.

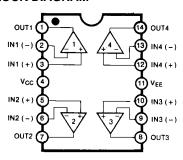
Other features include input offset currents and input bias current which are much less than those of a standard LM741. Also, excellent isolation between amplifiers has been achieved by independently biasing each amplifier and using layout techniques which minimize thermal coupling.

#### **FEATURES**

- LM741 OP Amp operating characteristics
- Low supply current drain
- Class AB output stage-no crossover distortion
- Pin compatible with the LM324 & LM3403
- Low input offset voltage: 1mV Typ.
- Low input offset current: 4nA Typ.
- · Low input bias current: 30nA Typ.
- Gain bandwidth product for LM348 (unity gain): 1.0MHz Typ.
- High degree of isolation between amplifiers: 120dB
- · Overload protection for inputs and outputs

# 41. Also, excellent isolation dependently biasing each minimize thermal coupling. 14 SOP 14 SOP

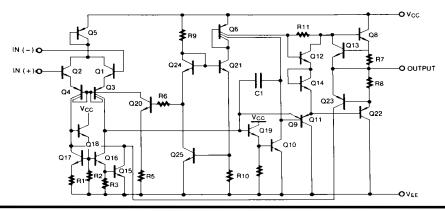
#### **BLOCK DIAGRAM**



#### **ORDERING INFORMATION**

Device	Package	Operating Temperature
LM348N	14 DIP	0 .70°C
LM348M	14 SOP	0 ~ +70°C
LM248N	14 DIP	
LM248M	14 SOP	-25 ~ +85 °C

#### SCHEMATIC DIAGRAM (One Section Only)





#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^{\circ}C$ )

Characteristic	Symbol	Value	Unit
Supply Voltage	V <sub>cc</sub>	±18	V
Differential Input Voltage	$V_{I(DIFF)}$	36	V
Input Voltage	Vi	±18	V
Output Short Circuit Duration		Continuous	
Operating Temperature KA248	T <sub>OPR</sub>	- 25 ~ +85	°C
KA348		0~ +70	°C
Storage Temperature	T <sub>STG</sub>	- 65~ +150	°C

#### **ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub> =15V, V<sub>EE</sub>= -15V,  $T_A$ =25 °C, unless otherwise specified)

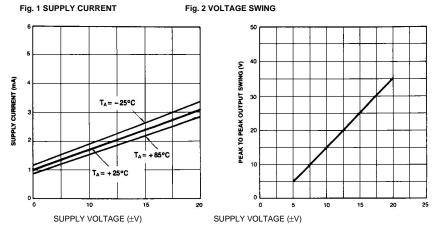
Characteristic	Cumhal	Took Co.	nditions		LM248	}		LM348	Unit		
Characteristic	Symbol	lest Co	naitions	Min	Тур	Max	Min	Тур	Max	Unit	
Innuit Officet Voltage	\/	R <sub>S</sub> ≤10KΩ			1	6.0		1	6.0	mV	
Input Offset Voltage	V <sub>IO</sub>		NOTE 1			7.5			7.5	IIIV	
Input Offset Current	1				4	50		4	50	nA	
input Onset Current	I <sub>IO</sub>		NOTE 1			125			100	IIA	
Input Bias Current	I <sub>BIAS</sub>				30	200		30	200	nA	
input bias current	BIAS		NOTE 1			500			400	ш	
Input Resistance	R <sub>I</sub>			0.8	2.5		8.0	2.5		$M\Omega$	
Supply Current (all Amplifiers)	Icc				2.4	4.5		2.4	4.5	mA	
Large Signal Voltage Gain	$G_V$	R₁≥2KΩ		25	160		25	160		V/mV	
		_	NOTE 1	15			15				
Channel Separation	CS	f = 1KHz to 2	0KHz		120			120		dB	
Common Mode Input Voltage Range	$V_{I(R)}$	NOTE 1		±12			±12			V	
Small Signal Bandwidth	BW	G <sub>V</sub> = 1			1.0			1.0		MHz	
Phase Margin	MPH	G <sub>V</sub> = 1			60			60		Degree	
Slew Rate	SR	G <sub>V</sub> = 1			0.5			0.5		V/μs	
Output Short Circuit Current	I <sub>sc</sub>				25			25		mA	
Output Voltage Swing	V <sub>O(P,P)</sub>	R <sub>L</sub> ≥10KΩ	NOTE 1	±12	±13		±12	±13			
Output Voltage Swing	V O(P.P)	R <sub>L</sub> ≥2KΩ	INOILI	±10	±12		+0	±12		V	
Common Mode Rejection Ratio	CMRR	R <sub>S</sub> ≥10KΩ	NOTE 1	70	90		70	90		dB	
Power Supply Rejection Ratio	PSRR	R <sub>S</sub> ≥10KΩ	NOTE 1	77	96		77	96		dB	

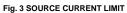
NOTE 1

 $LM348:~0 \leq T_A \leq +70^{\circ}C$   $LM248:~-25 \leq T_A \leq +85^{\circ}C$ 



#### **TYPICAL PERFORMANCE CHARACTERISTICS**





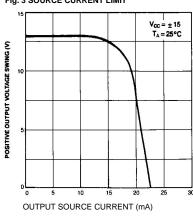
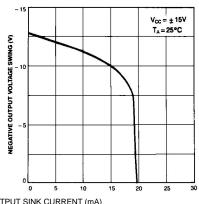
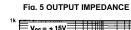
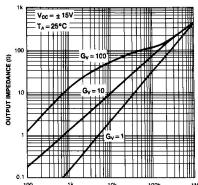


Fig. 4 SINK CURRENT LIMIT



OUTPUT SINK CURRENT (mA)





#### Fig. 6 COMMON-MODE REJECTION RATIO

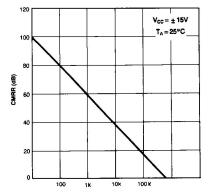




Fig. 7 OPEN LOOP FREGUENCV RESPONSE

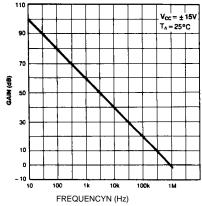


Fig. 8 BODE PLOT

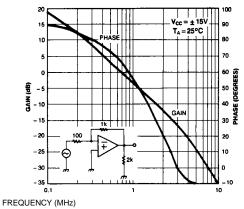
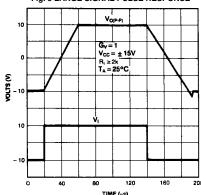


Fig. 9 LARGE SIGNAL PULSE RESPONSE



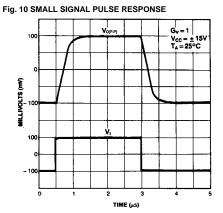


Fig. 11 UNDISTORTED OUTPUT VOLTAGE SWING

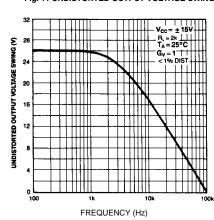
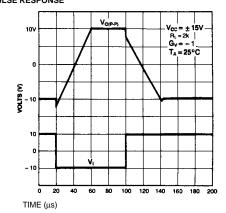


Fig. 12 INVERTING LARGE SIGNAL **PULSE RESPONSE** 



FAIRCHILD

SEMICONDUCTOR TM

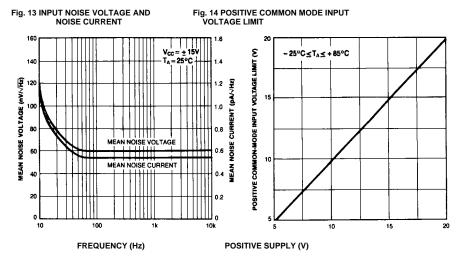
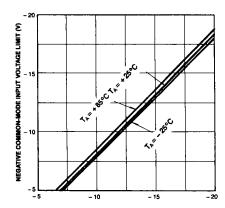


Fig. 15 NEGATIVE COMMON.MODE INPUT VOLTAGE LIMFY



NEGATIVE SUPPLY VOLTS(V)



#### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

#### **PRODUCT STATUS DEFINITIONS**

#### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

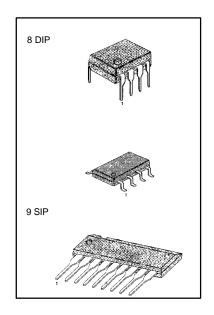
#### **DUAL OPERATIONAL AMPLIFIERS**

The LM258 series consists of four independent, high gain, internally Frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltage.

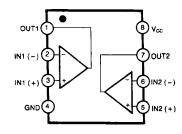
Operation from split power supplies is also possible and the low power Supply current drain is independent of the magnitude of the power Supply voltage. Application areas include transducer amplifier, DC gain blocks and all the conventional OP amp circuits which now can be easily implemented in single 8 SOP power supply system.

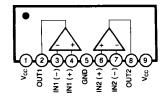
#### **FEATURES**

- Internally frequency compensated for unity gain
- Large DC voltage gain: 100dB
- Wide power supply range: LM258/A, LM358/A: 3V~32V (or ±1.5V~16V) LM2904: 3V~26V (or ±1.5V~13V)
- Input common-mode voltage range Includes ground
- Large output voltage swing: 0V DC to Vcc 1.5V DC
- · Power drain suitable for battery operation.

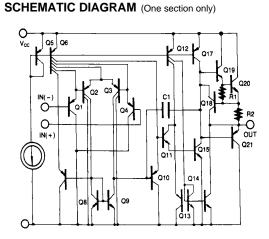


#### **BLOCK DIAGRAM**





# ORDERING INFORMATION



Device	Package	Operating Temperature
LM358N	8 DIP	
LM358AN	0 DIF	
LM358S	9 SIP	0 ~ + 70°C
LM358AS	9 31	0~+70 C
LM358M	8 SOP	
LM358AM	0 30F	
LM258N	8 DIP	
LM258AN	0 DIF	
LM258S	9 SIP	-25 ~ + 85 °C
LM258AS	9 31	-23 ~ + 65 C
LM258M	8 SOP	
LM258AM	8 301	
LM2904N	8 DIP	
LM2904S	9 SIP	-40 ~ + 85 °C
LM2904M	8 SOP	



#### **ABSOLUTE MAXIMUM RATINGS**

Characteristic	Symbol	LM258/LM258A	LM358/LM358A	LM2904	Unit
Supply Voltage	V <sub>CC</sub>	±16 or 32	±16 or 32	±13 or 26	V
Differential Input Voltage	$V_{I(DIFF)}$	32	32	26	V
Input Voltage	$V_{I}$	-0.3 to +32	-0.3 to +32	-0.3 to +26	V
Output Short Circuit to GND		Continuous	Continuous	Continuous	
V <sub>CC</sub> ≤V, T <sub>A</sub> = 25 °C(One Amp)		Continuous	Continuous	Continuous	
Operating Temperature Range	$T_{OPR}$	-25 ~ + 85	0 ~ + 70	-40 ~ + 85	°C
Storage Temperature Range	$T_{STG}$	-65 ~ + 150	-65 ~ + 150	-65 ~ + 150	°C

#### **ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub> = 5.0V, V<sub>EE</sub> = GND, T = 25  $^{\circ}$ C, unless otherwise specified)

01		Tool Conditions		LM25	8	ı	_M358	3	I	Unit		
Characteristic	Symbol	Test Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Input Offset Voltage	V <sub>IO</sub>	$V_{CM} = 0V \text{ to } V_{CC} - 1.5V$ $V_{O(P)} = 1.4V, R_S = 0\Omega$		2.9	5.0		2.9	7.0		2.9	7.0	mV
Input Offset Current	I <sub>IO</sub>			3	30		5	50		5	50	nA
Input Bias Current	I <sub>BIAS</sub>			45	150		45	250		45	250	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	$V_{CC} = 30V$ (KA2904, $V_{CC} = 26V$ )	0		V <sub>CC</sub> -1.5	0		V <sub>CC</sub> -1.5	0		V <sub>CC</sub> -1.5	V
Supply Current	Icc	$R_L = \infty$ , $V_{CC} = 30V$ (KA2902, $V_{CC} = 26V$ )		0.8	2.0		0.8	2.0		0.8	2.0	mA
		R <sub>L</sub> = ∞,over full temperature range		0.5	1.2		0.5	1.2		0.5	1.2	mA
Large Signal Voltage Gain	G <sub>V</sub>	$V_{CC} = 15V, R_L \ge 2K\Omega$ $V_{O(P)} = 1V \text{ to } 11V$	50	100		25	100		25	100		V/mV
	V <sub>O(H)</sub>	$V_{CC} = 30V$ $R_L = 2K\Omega$	26			26			22			V
Output Voltage Swing	V <sub>O(L)</sub>	$V_{CC} = 26V \text{ for } 2904  R_L = 10K\Omega$	27	28		27	28		23	24		V
	V O(L)	$V_{CC} = 5V, R_L \ge 10K\Omega$		5	20		5	20		5	100	mV
Common-Mode Rejection Ratio	CMRR		70	85		65	80		50	80		dB
Power Supply Rejection Ratio	PSRR		65	100		65	100		50	100		dB
Channel Separation	CS	f = 1KHz to 20KHz		120			120			120		dB
Short Circuit to GND	I <sub>SC</sub>			40	60		40	60		40	60	mA
	I <sub>SOURCE</sub>	$V_{I(+)} = 1V, V_{I(-)} = 0V$ $V_{CC} = 15V, V_{O(P)} = 2V$	10	30		10	30		10	30		mA
Output Current	I <sub>SINK</sub>	$V_{I(+)} = 0V, V_{I(-)} = 1V$ $V_{CC} = 15V, V_{O(P)} = 2V$	10	15		10	15		10	15		mA
		$V_{I(+)} = 0V, V_{I(-)} = 1V$ $V_{CC} = 15V, V_{O(P)} = 200mA$	12	100		12	100					μА
Differential Input Voltage	V <sub>I(DIFF)</sub>				V <sub>cc</sub>			V <sub>cc</sub>			V <sub>cc</sub>	V



#### **ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub>=5.0V, V<sub>EE</sub>=GND, unless otherwise specified) The following specification apply over the range of - 25 °C  $\leq$  T<sub>A</sub>  $\leq$  + 85 °C for the KA258; and the 0 °C  $\leq$  T<sub>A</sub>  $\leq$  + 70 °C for the LM358; and the -40 °C  $\leq$  T<sub>A</sub>  $\leq$  +85 °C for the LM2904

01	0	T O !!	Test Conditions		LM258			LM35	8	L	M290	Unit	
Characteristic	Symbol	l est Condi	tions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
Input Offset Voltage	V <sub>IO</sub>	$V_{CM} = 0V \text{ to } V_{CC} = 1.5$ $V_{O(P)} = 1.4V, R_S = 0C$				7.0			9.0			10.0	mV
Input Offset Voltage Drift	V <sub>IO</sub>	$R_S = 0\Omega$			7.0			7.0			7.0		μV/°C
Input Offset Current	I <sub>IO</sub>					100			150		45	200	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$				10			10			10		pA/°C
Input Bias Current	I <sub>BIAS</sub>				40	300		40	500		40	500	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	$V_{CC} = 30V$ (KA2904, $V_{CC} = 26V$ )		0		V <sub>CC</sub> =2.0	0		V <sub>CC</sub> =2.0	0		V <sub>CC</sub> =2.0	V
Large Signal Voltage Gain	$G_{V}$	$V_{CC} = 15V, R_L \ge 2.0K\Omega$ $V_{O(P)} = 1V \text{ to } 11V$	2	25			15			15			V/mV
	V <sub>O(H)</sub>	$V_{CC} = 30V$	$R_L = 2K\Omega$	26			26			26			V
Output Voltage Swing	V O(H)	V <sub>CC</sub> = 26V for 2904	$R_L = 10K\Omega$	27	28		27	28		27	28		V
	$V_{O(L)}$	V <sub>CC</sub> = 5V, R <sub>L</sub> ≥10KΩ			5	20		5	20		5	20	mV
Outrout Current	I <sub>SOURCE</sub>	$V_{I(+)} = 1V, V_{I(-)} = 0V$ $V_{CC} = 15V, V_{O(P)} = 2V$	/	10	30		10	30		10	30		mA
Output Current	I <sub>SINK</sub>	$V_{I(+)} = 0V, V_{I(-)} = 1V$ $V_{CC} = 15V, V_{O(P)} = 2V$	/	5	8		5	9		5	9		mA
Differential Input Voltage	V <sub>I(DIFF)</sub>					V <sub>cc</sub>			V <sub>cc</sub>			V <sub>cc</sub>	V



#### **ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub> = 5.0V. V<sub>EE</sub>=GND.  $T_A$ =25 °C, unless otherwise specified)

	Symbol		LM258A			LM358A			Unit
Characteristic		Test Conditions		Тур	Max	MIn	Тур	Max	Unit
Input Offset Voltage	V <sub>IO</sub>	$V_{CM} = 0V \text{ to } V_{CC} = 1.5V$ $V_{O(P)} = 1.4V, R_S = 0\Omega$		1.0	3.0		2.0	3.0	mV
Input Offset Current	I <sub>IO</sub>			2	15		5	30	nA
Input Bias Current	I <sub>BIAS</sub>			40	80		45	100	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	V <sub>CC</sub> = 30V	0		V <sub>CC</sub> =1.5	0		V <sub>CC</sub> =1.5	V
Supply Current	Icc	$R_L = \infty, V_{CC} = 30V$		8.0	2.0		8.0	2.0	mA
		RL = ∞,over full temperature range		0.5	1.2		0.5	1.2	mA
Large Signal Voltage Gain	Gv	$V_{CC}$ = 15V, $R_L \ge 2K\Omega$ $V_O$ = 1V to 11V	50	100		25	100		V/mV
Output Voltage Swing	V <sub>OH</sub>	$V_{CC} = 30V$ $R_L = 2K\Omega$	26			26			V
		$V_{CC} = 26V \text{ for } 2904  R_L = 10K\Omega$	27	28		27	28		V
	V <sub>O(L)</sub>	V <sub>CC</sub> = 5V, R <sub>L</sub> ≥10KΩ		5	20		5	20	mV
Common-Mode Rejection Ratio	CMRR		70	85		65	85		dB
Power Supply Rejection Ratio	PSRR		65	100		65	100		dB
Channel Separation	CS	f = 1KHz to 20KHz		120			120		dB
Short Circuit to GND	I <sub>sc</sub>			40	60		40	60	mA
Output Current	I <sub>SOURCE</sub>	$V_{I(+)} = 1V, V_{I(-)} = 0V$ $V_{CC} = 15V, V_{O(P)} = 2V$	20	30		20	30		mA
	I <sub>SINK</sub>	$V_{I(+)} = 1V, V_{I(-)} = 0V$ $V_{CC} = 15V, V_{O(P)} = 2V$	10	15		10	15		mA
		$V_{in+} = 0V, V_{in-} = 1V$ $V_{O(P)} = 200mV$	12	100		12	100		μА
Differential Input Voltage	$V_{I(DIFF)}$	_			$V_{CC}$			$V_{CC}$	V



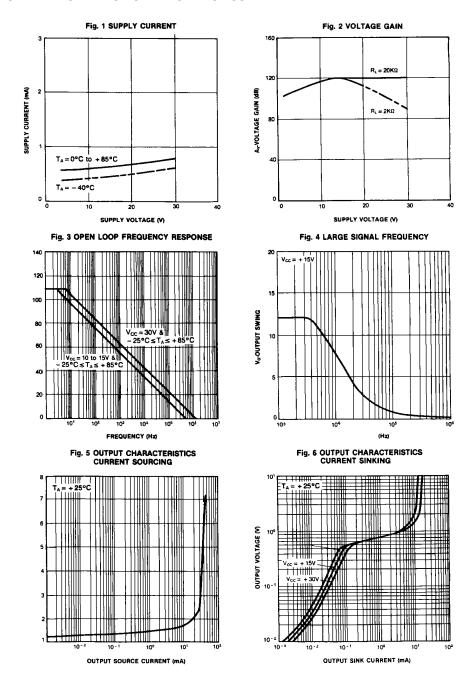
#### **ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 5.0V$ , $V_{EE} = GND$ . unless otherwise specified)

The following specification apply over the range of -25  $^{\circ}$ C  $\leq$  T  $_{A}$   $\leq$  +85  $^{\circ}$ C for the LM258A; and the 0  $^{\circ}$ C  $\leq$  T  $_{A}$   $\leq$  +70  $^{\circ}$ C for the LM358A

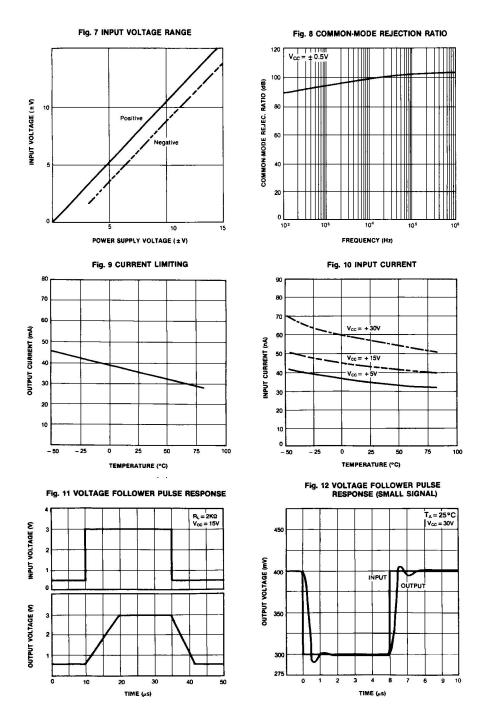
Characteristic	Symbol	Test Conditions		LM258A			LM358A			
				Min	Тур	Max	Min	Тур	Max	Unit
Input Offset Voltage	V <sub>IO</sub>	$V_{CM} = 0V$ to $V_{CC} = 1.5V$ $V_{O(P)} = 1.4V$ , $R_S = 0\Omega$				4.0			5.0	mV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$				7.0	15		7.0	20	μV/°C
Input Offset Current	I <sub>IO</sub>					30			75	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$				10	200		10	300	pA/°C
Input Bias Current	I <sub>BIAS</sub>				40	100		40	200	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	V <sub>CC</sub> = 30V		0		Vcc =2.0	0		Vcc =2.0	V
Output Voltage Swing	V <sub>O(H)</sub>	$V_{CC} = 30V$	$R_L = 2K\Omega$	26			26			V
		$V_{CC} = 30V$	$R_L = 10K\Omega$	27	28		27	28		V
	V <sub>O(L)</sub>	$V_{CC} = 5V, R_L$		5	20		5	20	mV	
Large Signal Voltage Gain	G <sub>V</sub>	$V_{CC} = 15V$ , $R_L \ge 2.0 K\Omega$ $V_{O(P)} = 1V$ to 11V		25			15			V/mV
Output Current	I <sub>SOURCE</sub>	$V_{I(+)} = 1V, V_{I(-)} = 0V$ $V_{CC} = 15V, V_{O(P)} = 2V$		10	30		10	30		mA
	I <sub>SINK</sub>	$V_{I(+)} = 1V, V_{I(-)} = 0V$ $V_{CC} = 15V, V_{O(P)} = 2V$		5	9		5	9		mA
Differential Input Voltage	$V_{I(DIFF)}$					$V_{CC}$			$V_{CC}$	V



#### **TYPICAL PERFORMANCE CHARACTERISTICS**









The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## **PRODUCT STATUS DEFINITIONS**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

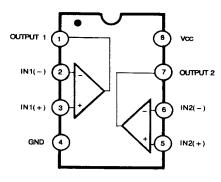
## **DUAL DIFFERENTIAL COMPARATOR**

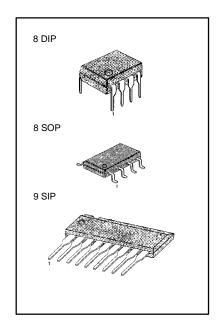
The LM/KA293 series consists of two independent voltage comparators designed to operate from a single power supply over a wide voltage

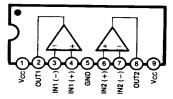
# **FEATURES**

- Single Supply Operation: 2V to 36V
- Dual Supply Operation: ± 1V to ±18V
- Allow Comparison of Voltages Near Ground Potential
   Low Current Drain 800μA Typ
- Compatible with all Forms of Logic
- Low Input Bias Current 25nA Typ
   Low Input Offset Current ±5nA WP
- Low Offset Voltage ±1mV Typ

# **BLOCK DIAGRAM**





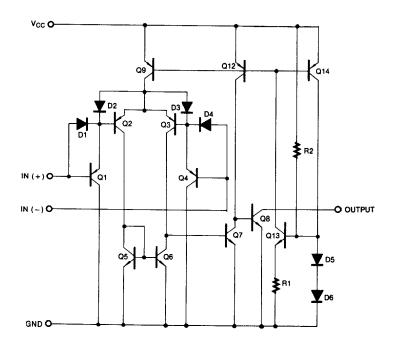


# **ORDERING INFORMATION**

Device	Package	Operating Temperature
LM393N (KA393) LM393AN (KA393A)	8 DIP	
KA393S KA393AS	9 SIP	0 ~ + 75°C
LM393M (KA393D) KA393AD	8 SOP	
KA293 KA293A	8 DIP	
KA293S KA293AS	9 DIP	-25 ~ + 85°C
KA293D KA293AD	8 SOP	
KA2903	8 DIP	
KA2903D	8 SOP	-40 ~ + 85°C
KA2903S	9 SIP	



# **SCHEMATIC DIAGRAM**



# **ABSOLUTE MAXIMUM RATINGS**

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V <sub>CC</sub>	±18 or 36	V
Differential Input Voltage	$V_{I(DIFF)}$	36	V
Input Voltage	V <sub>I</sub>	- 0.3 to +36	V
Output Short Circuit to GND		Continuous	
Power Dissipation	P <sub>D</sub>	570	mW
Operating Temperature LM393/LM393A LM293/LM293A LM2903	T <sub>OPR</sub>	0 ~ + 70 - 25 ~ + 85 - 40 ~ + 85	°C
Storage Temperature	T <sub>STG</sub>	- 65 ~ + 150	°C



# **ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> =5V, T<sub>A</sub>=25°C, unless otherwise specified)

		Test Conditions		LM2	93A/L	M393A	LM293/LM393			11
Characteristic	Symbol			Min	Тур	Max	Min	Тур	Max	Unit
Innut Offeet Veltege	V <sub>IO</sub>	$V_{CM} = 0V$ to $V_{CC} = 1.5V$			±1	±2		±1	±5	
Input Offset Voltage	VIO	$V_{O(P)} = 1.4V, R_S = 0\Omega$	NOTE 1			±4.0			±9.0	mV
	I <sub>IO</sub>				±5	±50		±5	±50	Λ
Input Offset Current	10		NOTE 1			±150			±150	nA
Input Bias Current	laa				65	250		65	250	nA
Input bias outront	I <sub>BIAS</sub>		NOTE 1			400			400	IIA
Input Common Mode	$V_{I(R)}$			0		V <sub>CC</sub> -1.5	0		V <sub>CC</sub> -1.5	V
Voltage Range	- 1(10)		NOTE 1	0		V <sub>CC</sub> -2	0		V <sub>CC</sub> -2	•
Supply Current	lcc	R <sub>L</sub> = ∞			0.6	1		0.6	1	mA
опрріу оппені	ICC	$R_L = \infty$ , $V_{CC} = 30V$			0.8	2.5		0.8	2.5	1117 (
Voltage Gain	$G_V$	V <sub>CC</sub> =15V, R <sub>L</sub> ≥15KΩ (fe	or large V <sub>O(P-P)swing</sub> )	50	200		50	200		V/mV
Large Signal Response Time	t <sub>RES</sub>	$V_I$ =TTL Logic Swing $V_{REF}$ =1.4V, $V_{RL}$ =5V, F	R <sub>L</sub> =5.1KΩ		350			350		ns
Response Time	t <sub>RES</sub>	$V_{RL}$ =5V, $R_L$ =5.1K $\Omega$			1.4			1.4		μs
Output Sink Current	I <sub>SINK</sub>	V <sub>I(-)</sub> ≥1V, V <sub>I(+)</sub> =0V, V <sub>O(P</sub>	$V_{I(-)} \ge 1V$ , $V_{I(+)} = 0V$ , $V_{O(P)} \le 1.5V$		18		6	18		mA
Output Caturation Valtage	V <sub>SAT</sub>	V <sub>I(-)</sub> ≥1V, VI(+) =0V			160	400		160	400	\/
Output Saturation Voltage	▼ SAT	I <sub>SINK</sub> = 4mA	NOTE 1			700			700	mV
Output Leakage Current	I <sub>O(LKG)</sub>	$V_{I(-)} = 0V$ ,	$V_{O(P)} = 5V$		0.1			0.1		nA
Carpar Ecanage Current	iO(LKG)	$V_{I(+)} = 1V$	$V_{O(P)} = 30V$			1.0			1.0	μΑ

NOTE 1

 $\begin{array}{l} LM393/A:\ 0{\le}T_A{\le} +70^{\circ}C \\ LM293/A:\ -25{\le}T_A{\le} +85^{\circ}C \\ LM2903:\ -40{\le}T_A{\le} +85^{\circ}C \end{array}$ 



# **ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> =5V, T<sub>A</sub>=25°C, unless otherwise specified)

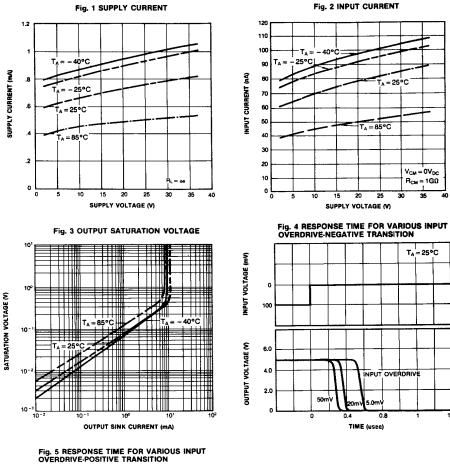
Characteristic	Sumbol	Symbol			LM2903			
Characteristic	Symbol	Test Conditions		Min	Тур	Max	Unit	
		$V_{CM} = 0V$ to $V_{CC} = 1.5V$			±1	±7	.,	
Input Offset Voltage	V <sub>IO</sub>	$V_{O(P)} = 1.4V, R_S = 0\Omega$	NOTE 1		±9	±15	mV	
Innut Officet Current					±5	±50	nA	
Input Offset Current	I <sub>IO</sub>		NOTE 1		±50	±200	nA	
Input Bias Current	I <sub>BIAS</sub>				65	250	nA	
Input bias Current	BIAS		NOTE 1			500	ш	
Input Common Mode	V <sub>I(R)</sub>			0		V <sub>CC</sub> -1.5	V	
Voltage Range	VI(R)		NOTE 1	0		V <sub>CC</sub> -2	2 v	
Supply Current		R <sub>L</sub> = ∞			0.6	1		
Supply Current	Icc	$R_L = \infty$ , $V_{CC} = 30V$			1	2.5	mA	
Voltage Gain	$G_V$	V <sub>CC</sub> =15V, R <sub>L</sub> ≥15KΩ(fc	or large V <sub>O(P-P)swing</sub> )	25	100		V/mV	
Large Signal Response Time	t <sub>RES</sub>	$V_I = TTL Logic Swing$ $V_{REF} = 1.4V$ , $V_{RL} = 5V$ , F	R <sub>L</sub> =5.1KΩ		350		ns	
Response Time	t <sub>RES</sub>	$V_{RL}$ =5V, $R_L$ =5.1K $\Omega$			1.5		μs	
Output Sink Current	I <sub>SINK</sub>	V <sub>I(-)</sub> ≥1V, V <sub>I(+)</sub> =0V, V <sub>O(P</sub>	<sub>2)</sub> ≤1.5V	6	16		mA	
Output Saturation Voltage	V <sub>SAT</sub>	V <sub>I(-)</sub> ≥1V, VI(+) =0V			160	400		
Output Saturation voltage	V SAT	I <sub>SINK</sub> = 4mA	NOTE 1			700	mV	
Output Leakage Current	I <sub>O(LKG)</sub>	$V_{I(-)} = 0V$ ,	$V_{O(P)} = 5V$		0.1		nA	
Output Leakage Current	iO(LKG)	$V_{I(+)} = 1V$	$V_{O(P)} = 30V$			1.0	μΑ	

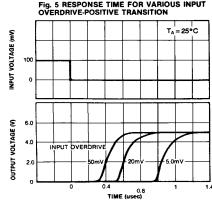
NOTE 1

LM393/A: 0≤T<sub>A</sub>≤ +70°C LM293/A: -25≤T<sub>A</sub>≤ +85°C LM2903: -40≤T<sub>A</sub>≤ +85°C



# TYPICAL PERFORMANCE CHARACTERISTICS







The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

 $E^2CMOS^{TM}$  PowerTrench® FACT Quiet Series QSTM QSTM

 $\begin{array}{lll} \mathsf{FAST}^{\circledR} & \mathsf{Quiet} \; \mathsf{Series^{\intercal M}} \\ \mathsf{FASTr^{\intercal M}} & \mathsf{SuperSOT^{\intercal M}\text{--}3} \\ \mathsf{GTO^{\intercal M}} & \mathsf{SuperSOT^{\intercal M}\text{--}6} \\ \mathsf{HiSeC^{\intercal M}} & \mathsf{SuperSOT^{\intercal M}\text{--}8} \\ \end{array}$ 

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

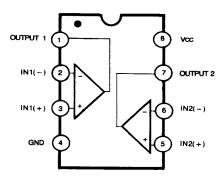
# **DUAL DIFFERENTIAL COMPARATOR**

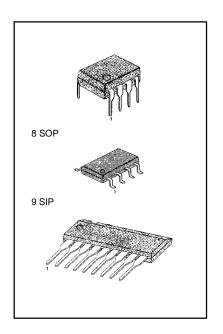
The LM293 series consists of two independent voltage comparators designed to operate from a single power supply over a wide voltage

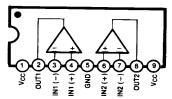
# **FEATURES**

- Single Supply Operation: 2V to 36V
   Dual Supply Operation: ± 1V to ±18V
   Allow Comparison of Voltages Near Ground Potential
- Low Current Drain 800μA Typ
- Compatible with all Forms of Logic
- Low Input Bias Current 25nA Typ
   Low Input Offset Current ±5nA WP
- Low Offset Voltage ±1mV Typ

# **BLOCK DIAGRAM**





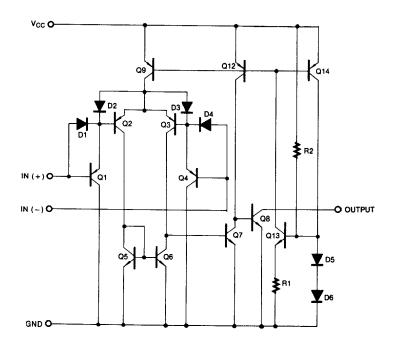


# **ORDERING INFORMATION**

Device	Package	Operating Temperature
LM393N LM393AN	8 DIP	
LM393S LM393AS	9 SIP	0 ~ + 75°C
LM393M LM393AM	8 SOP	
LM293N LM293AN	8 DIP	
LM293S LM293AS	9 DIP	-25 ~ + 85°C
LM293M LM293AM	8 SOP	
LM2903N	8 DIP	
LM2903M	8 SOP	-40 ~ + 85°C
LM2903S	9 SIP	



# **SCHEMATIC DIAGRAM**



# **ABSOLUTE MAXIMUM RATINGS**

Characteristic	Symbol	Value	Unit
Power Supply Voltage	V <sub>cc</sub>	±18 or 36	V
Differential Input Voltage	$V_{I(DIFF)}$	36	V
Input Voltage	$V_{l}$	- 0.3 to +36	V
Output Short Circuit to GND		Continuous	
Power Dissipation	$P_D$	570	mW
Operating Temperature LM393/LM393A LM293/LM293A LM2903	T <sub>OPR</sub>	0 ~ + 70 - 25 ~ + 85 - 40 ~ + 85	°C
Storage Temperature	T <sub>STG</sub>	- 65 ~ + 150	°C



# **ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> =5V, T<sub>A</sub>=25°C, unless otherwise specified)

01		mbol Test Conditions		LM2	LM293A/LM393A			LM293/LM393		
Characteristic	Symbol			Min	Тур	Max	Min	Тур	Max	Unit
Inn t Off t \ / -   t	.,	$V_{CM} = 0V$ to $V_{CC} = 1.5V$			±1	±2		±1	±5	
Input Offset Voltage	V <sub>IO</sub>	$V_{O(P)} = 1.4V, R_S = 0\Omega$	NOTE 1			±4.0			±9.0	mV
	l				±5	±50		±5	±50	^
Input Offset Current	I <sub>IO</sub>		NOTE 1			±150			±150	nA
Input Bias Current					65	250		65	250	nA
input bias Current	I <sub>BIAS</sub>		NOTE 1			400			400	IIA
Input Common Mode	V <sub>I(R)</sub>			0		V <sub>CC</sub> -1.5	0		V <sub>CC</sub> -1.5	V
Voltage Range	• 1(10)	NOTE 1		0		V <sub>CC</sub> -2	0		V <sub>CC</sub> -2	v
Supply Current		R <sub>L</sub> = ∞			0.6	1		0.6	1	mA
Supply Current	Icc	$R_L = \infty$ , $V_{CC} = 30V$			8.0	2.5		8.0	2.5	ША
Voltage Gain	$G_V$	$V_{CC}$ =15V, $R_L \ge 15K\Omega$ (f	or large V <sub>O(P-P)swing</sub> )	50	200		50	200		V/mV
Large Signal Response Time	t <sub>RES</sub>	$V_I$ =TTL Logic Swing $V_{REF}$ =1.4V, $V_{RL}$ =5V, F	R <sub>L</sub> =5.1KΩ		350			350		ns
Response Time	t <sub>RES</sub>	$V_{RL}$ =5V, $R_L$ =5.1K $\Omega$			1.4			1.4		μs
Output Sink Current	I <sub>SINK</sub>	$V_{I(-)} \ge 1V$ , $V_{I(+)} = 0V$ , $V_{O(P)}$	<sub>')</sub> ≤1.5V	6	18		6	18		mA
Output Saturation Voltage V <sub>SAT</sub>		$V_{ (-)} \ge 1V$ , $V_{ (+)} = 0V$			160	400		160	400	.,
Output Saturation Voltage	V SAT	I <sub>SINK</sub> = 4mA	NOTE 1			700			700	mV
Output Leakage Current	I <sub>O(LKG)</sub>	$V_{I(-)} = 0V$ ,	$V_{O(P)} = 5V$		0.1			0.1		nA
Output Leakage Current	'O(LKG)	$V_{I(+)} = 1V$	$V_{O(P)} = 30V$			1.0			1.0	μΑ

NOTE 1

LM393/A: 0≤T<sub>A</sub>≤ +70°C LM293/A: -25≤T<sub>A</sub>≤ +85°C LM2903: -40≤T<sub>A</sub>≤ +85°C



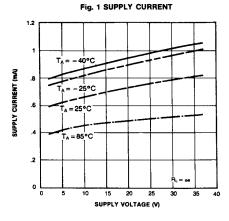
# $\textbf{ELECTRICAL CHARACTERISTICS} \; (V_{\text{CC}} = 5V, T_{\text{A}} = 25^{\circ}\text{C}, \text{ unless otherwise specified})$

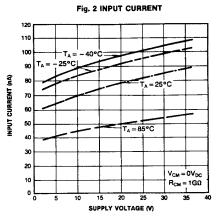
Characteristic	Characteristic Symbol		Total Constitution		LM2903			
Characteristic	Symbol	Test Conditions		Min	Тур	Max	Unit	
		$V_{CM} = 0V$ to $V_{CC} = 1.5V$			±1	±7	.,	
Innut Offset Voltage	V <sub>IO</sub>	$V_{O(P)} = 1.4V, R_S = 0\Omega$	NOTE 1		±9	±15	mV	
Innut Officet Current	lio				±5	±50	nA	
Input Offset Current	IIO		NOTE 1		±50	±200	ПА	
Input Bias Current	laura				65	250	nA	
Input bias Current	IBIAS		NOTE 1			500	IIA	
Input Common Mode	$V_{I(R)}$			0		V <sub>CC</sub> -1.5	V	
Voltage Range	VI(R)		NOTE 1	0		V <sub>CC</sub> -2	V	
Cumply Current		R <sub>L</sub> = ∞			0.6	1		
Supply Current	Icc	$R_L = \infty$ , $V_{CC} = 30V$			1	2.5	mA	
Voltage Gain	$G_V$	V <sub>CC</sub> =15V, R <sub>L</sub> ≥15KΩ(fo	r large V <sub>O(P-P)swing</sub> )	25	100		V/mV	
Large Signal Response Time	t <sub>RES</sub>	$V_I$ =TTL Logic Swing $V_{REF}$ =1.4V, $V_{RL}$ =5V, F	R <sub>L</sub> =5.1KΩ		350		ns	
Response Time	t <sub>RES</sub>	$V_{RL}$ =5V, $R_L$ =5.1K $\Omega$			1.5		μs	
Output Sink Current	I <sub>SINK</sub>	V <sub>I(-)</sub> ≥1V, V <sub>I(+)</sub> =0V, V <sub>O(P</sub>	<sub>)</sub> ≤1.5V	6	16		mA	
Output Saturation Voltage	V <sub>SAT</sub>	V <sub>I(-)</sub> ≥1V, VI(+) =0V			160	400	.,	
Output Saturation voltage	V SAT	I <sub>SINK</sub> = 4mA	NOTE 1			700	mV	
Output Leakage Current	1	$V_{I(-)} = 0V$ ,	$V_{O(P)} = 5V$		0.1		nA	
Output Leakage Current	I <sub>O(LKG)</sub>	$V_{I(+)} = 1V$	V <sub>O(P)</sub> = 30V			1.0	μΑ	

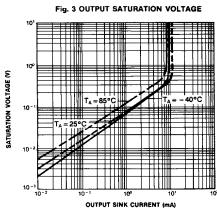
NOTE 1 LM393/A: 0≤T<sub>A</sub>≤ +70°C LM293/A: -25≤T<sub>A</sub>≤ +85°C LM2903: -40≤T<sub>A</sub>≤ +85°C

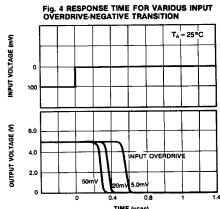


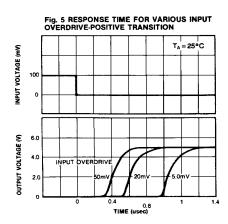
# **TYPICAL PERFORMANCE CHARACTERISTICS**











FAIRCHILD SEMICONDUCTOR TM

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## **PRODUCT STATUS DEFINITIONS**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

## **VOLTAGE COMPARATOR**

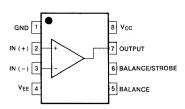
The LM311 series is a monolithic, low input current voltage comparator.

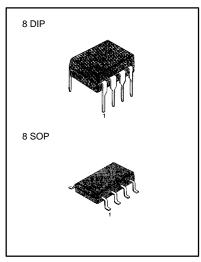
The device is also designed to operate from dual or single supplies voltage

#### **FEATURE**

- Low input bias current : 250nA (Max)
- Low input offset current : 50nA (Max)
- Differential Input Voltage: ±30V.
- Power supply voltage : single 5.0V supply to  $\pm 15$ V.
- Offset voltage null capability.
- Strobe capability.

# **BLOCK DIAGRAM**

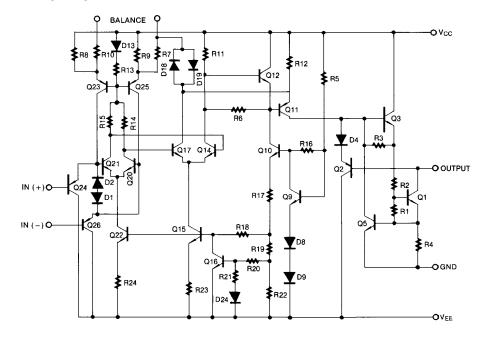




# **ORDERING IN FORMATION**

Device	Package	Operating Temperature
LM311N	8 DIP	0 ~ +70°C
LM311M	8 SOP	0~+70 C

# **SCHEMATIC DIAGRAM**





# **ABSOLUTE MAXIMUM RATINGS**

Characteristic	Symbol	Value	Unit
Total Supply Voltage	V <sub>CC</sub>	36	V
Output to Negative Supply Voltage KA311	Vo - VEE	40	V
Ground to Negative voltage	$V_{EE}$	-30	V
Differential Input Voltage	$V_{I(DIFF)}$	30	V
Input Voltage	$V_1$	±15	V
Output Short Circuit Duration		10	sec
Power Dissipation	$P_D$	500	mW
Operating Temperature Range	T <sub>OPR</sub>	0 ~ +70	°C
Storage Temperature Range	T <sub>STG</sub>	- 65 ~ <b>+</b> 150	°C

# **ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 15V$ , $T_A = 25$ °C, unless otherwise specified)

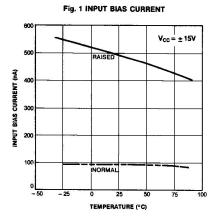
Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
Input Offset Voltage	.,	R <sub>S</sub> ≤50KΩ		1.0	7.5	\/
iliput Oliset voltage	V <sub>IO</sub>	NOTE 1			10	mV
Input Offset Current	I <sub>IO</sub>			6	50	nA
input Onset Current	טוי	NOTE 1			70	ш
1 10 0				100	250	nA
Input Bias Current	I <sub>BIAS</sub>	NOTE 1			300	II/A
Voltage Gain	$G_V$		40	200		V/mV
Response Time	t <sub>RES</sub>	NOTE 2		200		ns
		I <sub>O</sub> =50mA, V <sub>I</sub> ≤-10mV		0.75	1.5	
Saturation Voltage	V <sub>SAT</sub>	$V_{CC} \ge 4.5 \text{V}, V_{EE} = 0 \text{V}$ $I_{SINK} = 8\text{mA}, V_{I} \ge -10\text{mV}, \text{NOTE 1}$		0.23	0.4	V
Strobe "NO" Current	I <sub>STR(ON)</sub>			3		mA
Output Leakage Current	I <sub>SINK</sub>	$I_{STR}$ =3mA, $V_1 \ge 10$ mV $V_{O(P)}$ =35V, $V_{EE}$ = $V_{GND}$ =-5V		0.2	50	nA
Input Voltage Range	V <sub>I(R)</sub>	NOTE 1	-14.5 to 13.0	-14.7 to 13.8		V
Positive Supply Current	Icc			3.0	7.5	mA
Negative Supply Current	I <sub>EE</sub>			-2.2	-5.0	mA
Strobe Current	I <sub>STR</sub>			3		mA

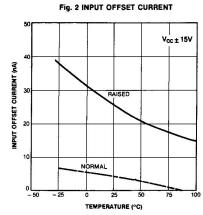
NOTE 1.  $0 \le T_A \le +70^{\circ}C$ 



<sup>2.</sup> The response time specified is for a 100mV input step with 5mV over drive.

# **TYPICAL PERFORMANCE CHARACTERISTICS**







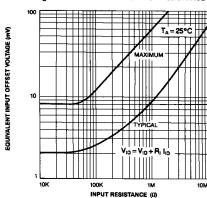


Fig. 4 INPUT BIAS CURRENT VS DIFFERENTIAL

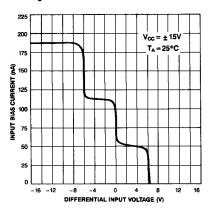


Fig. 5 COMMON MODE LIMITS VS TEMPERATURE

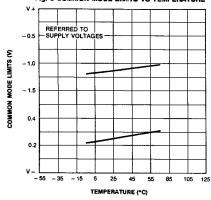
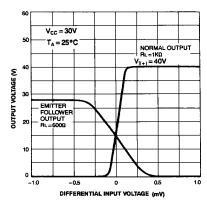
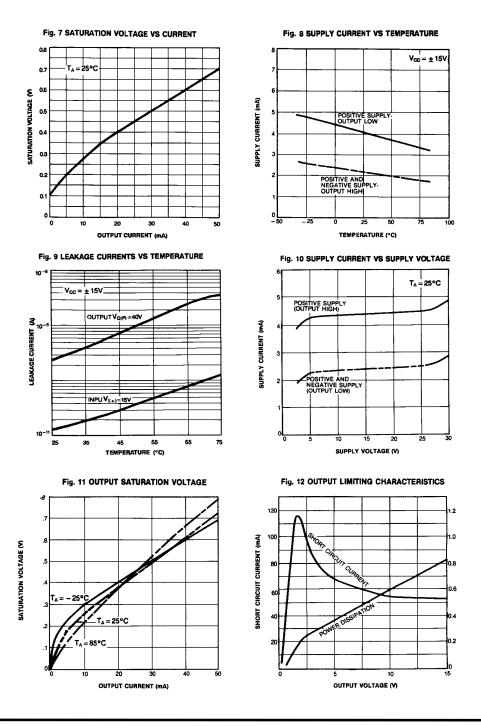


Fig. 6 OUTPUT VOLTAGE VS DIFFERENTIAL









The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

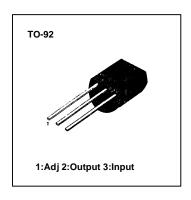
 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## **PRODUCT STATUS DEFINITIONS**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

# 3-TERMINAL 0.1A POSITIVE ADJUSTABLE REGULATOR

The LM317L is a 3-terminal adjustable positive voltage regulator capable of supplying in excess of 100mA over an output voltage range of 1.2V to 37V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage.



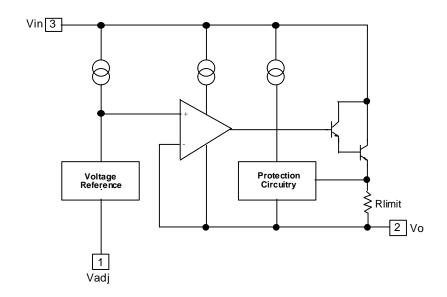
#### **FEATURES**

- Output current in excess of 100mA
- Output adjustable between 1.2V and 37V
- Internal thermal-overload protection
- Internal short-circuit current-limiting
- Output transistor safe-area compensation
- Floating operation for high-voltage applications

#### **ORDERING INFORMATION**

Device	Package	Operating Temperature
LM317LZ	TO-92	0 ~ 125°C

# **BLOCK DIAGRAM**





## **ABLOLUTE MAXIMUM RATINGS**

Characteristic	Symbol	Value	Unit
Input-Output Voltage Differential	V <sub>I</sub> - V <sub>O</sub>	40	V
Power Dissipation	$P_D$	Internally limited	W
Operating Temperature Range	$T_{OPR}$	0 ~ +125	°C
Storage Temperature Range	T <sub>STG</sub>	-65 ~+125	°C

# **ELECTRICAL CHARACTERISTICS**

(V<sub>I</sub> - V<sub>O</sub> = 5V, I<sub>O</sub> = 40mA,  $0^{\circ}$ C  $\leq$  T<sub>J</sub> $\leq$  +125 $^{\circ}$ C, P<sub>DMAX</sub> = 625mW, unless otherwise specified)

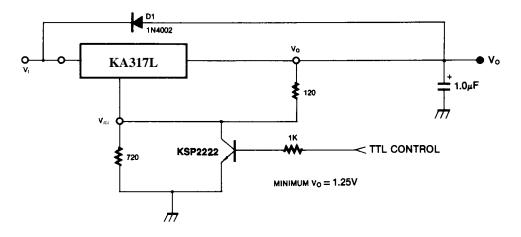
Characteristic	Characteristic Symbol Test Condit		Min	Тур	Max	Unit
*Line Regulation	ΔV <sub>O</sub>	$T_A = +25^{\circ}C$ $3V \le V_1 \le V_0 \le 40V$		0.01	0.04	%/V
		$3V \le V_1 \le V_0 \le 40V$		0.02	0.07	
		$T_A = +25^{\circ}C$ $10\text{mA} \le I_O \le 100\text{mA}$				
		$V_0 \le 5V$		5	25	mV
*Load Regulation	$\Delta V_{O}$	V <sub>O</sub> ≥5V		0.1	0.5	%/ V <sub>O</sub>
		$10mA \le I_O \le 100mA$ $V_O \le 5V$ $V_O \ge 5V$		20 0.3	70 1.5	mV %/ Vo
Adjustment Pin Current	I <sub>ADJ</sub>	10 = 01		50	100	μА
Adjustment Pin Current Change	$\Delta I_{ADJ}$	$3V \le V_1 - V_0 \le 40V$ $10mA \le I_0 \le 100mA$ $P_D < P_{DMAX}$		0.2	5	μА
Reference Voltage	$V_{REF}$	$3V < V_I - V_O < 40V$ $10mA \le I_O \le 100mA$ $P_D \le P_{DMAX}$	1.20	1.25	1.30	V
Temperature Stability	ST <sub>T</sub>			0.7		%
Minimum Load Current to Maintain Regulation	I <sub>L(MIN)</sub>	V <sub>I</sub> - V <sub>O</sub> = 40V		3.5	10	mA
		$V_1 - V_0 = 5V$ $P_D < P_{DMAX}$	100	200		
		$V_{I} - V_{O} = 40V$ $P_{D} < P_{DMAX}, T_{A} = +25^{\circ}C$	25	50		
RMS Noise, % of V <sub>OUT</sub>	e <sub>N</sub>	T <sub>A</sub> =+ 25°C 10Hz < f <10KHz		0.003		%/ V <sub>0</sub>
Ripple Rejection	RR	$V_O = 10V$ , $f = 120Hz$ without $C_{ADJ}$ $C_{ADJ} = 10\mu F$	66	65 80		dB
Long-Term Stability	ST	T <sub>J</sub> = +125 °C, 1000 Hours		0.3		%

 $<sup>^{\</sup>star}$  Load and Line regulation are specified at constant junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.



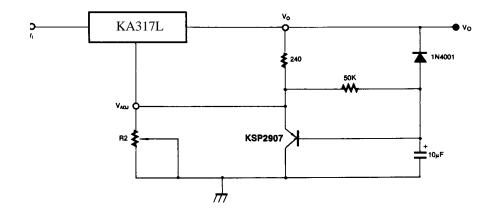
# **TYPICAL APPLICATIONS**

Fig. 1 5V Electronic Shutdown Regulator

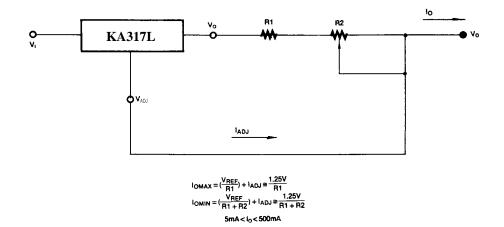


D1 protects the device during an input short circuit.

Fig. 2 Slow Turn-On Regulator

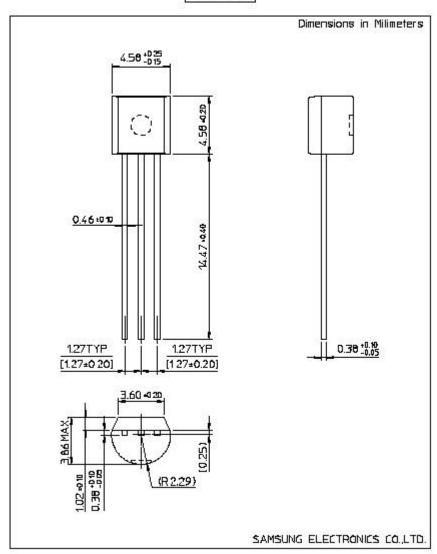














The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## **PRODUCT STATUS DEFINITIONS**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

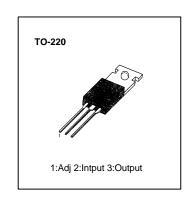
# LM337 (KA337) ADJUSTABLE VOLTAGE REGULATOR (NEGATIVE)

## 3-TERMINAL 1.5A NEGATIVE ADJUSTABLE REGULATOR

The LM337 is a 3-terminal negative adjustable regulator. It supply in excess of 1.5A over an output voltage range of -1.2V to -37V. This regulator requires only two external resistor to set the output voltage. Included on the chip are current limiting, thermal overload protection and safe area compensation.

## **FEATURES**

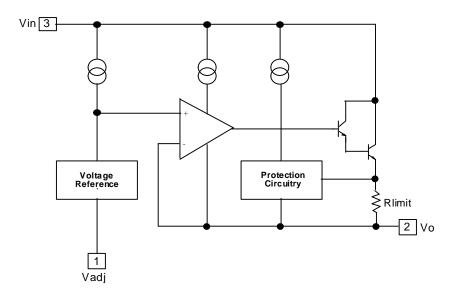
- Output current In excess of 1.5A
- Output voltage adjustable between -1.2V and 37V
- Internal thermal-overload protection
- Internal short-circuit current limiting
- Output transistor safe-area compensation
- Floating operation for high-voltage applications
- Standard 3-pin TO-220 package



## **ORDERING INFORMATION**

Device	Package	Operating Temperature
LM337T	TO-220	0 ~ + 125°C

# **BLOCK DIAGRAM**





# LM337 (KA337) ADJUSTABLE VOLTAGE REGULATOR (NEGATIVE)

# **ABSOLUTE MAXIMUM RATINGS**

Characteristic	Symbol	Value	Unit
Input-Output Voltage Differential	V <sub>I</sub> - V <sub>O</sub>	40	V
Power Dissipation	$P_D$	Internally limited	W
Operating Temperature Range	$T_{OPR}$	0 ~ +125	°C
Storage Temperature Range	T <sub>STG</sub>	-65 ~+125	°C

# **ELECTRICAL CHARACTERISTICS**

(V<sub>I</sub> - V<sub>O</sub> = 5V, I<sub>O</sub> = 40mA,  $0^{\circ}$ C  $\leq$  T<sub>J</sub> $\leq$  +125 $^{\circ}$ C, P<sub>DMAX</sub> = 20W, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
Line Regulation	Vo	$T_A = +25^{\circ}C$ - $40V \le V_O - V_I \le -3V$		0.01	0.04	%/ V
		- 40V ≤ V <sub>O</sub> - V <sub>I</sub> ≤ -3V		0.02	0.07	
Load Regulation	Vo	$T_A = +25^{\circ}C$ 10mA \leq I <sub>O</sub> \leq 0.5A		15	50	mV
		10mA ≤ I <sub>O</sub> ≤1.5A		15	150	
Adjustable Pin Current	I <sub>ADJ</sub>			50	100	μА
Adjustable Pin Current	$\Delta l_{ADJ}$	$T_A = + 25^{\circ}C$ $10mA \le I_O \le 1.5A$ $- 40V \le V_O - V_1 \le -3V$		2	5	μА
		T <sub>A</sub> =+ 25°C	-1.213	-1.250	-1.287	
Reference Voltage	$V_{REF}$	$-40V \le V_O - V_1 \le -3V$ $10mA \le I_O \le 1.5A$	-1.200	-1.250	-1.300	V
Temperature Stability	ST <sub>T</sub>			0.6		%
Minimum Load Current		- $40V \le V_O$ - $V_I \le -3V$		2.5	10	
to Maintain Rejection		$-10V \le V_{O} - V_{I} \le -3V$		1.5	6	mA
Output Noise	en	$T_A = +25^{\circ}C \ 10Hz \le f \le 10KHz$		3×V <sub>OUT</sub>		V/10 <sup>6</sup>
Ripple Rejection Ratio		$V_0 = -10V$ , $f = 120Hz$		60		
		$C_{ADJ} = 10 \mu F$	66	77		dB
Long Term Stability	ST	T <sub>J</sub> = 125°C ,1000Hours		0.3	1	%
Thermal Resistance Junction to Case	R <sub>EJC</sub>			4		°C/W

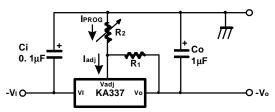
<sup>.</sup>  $^{\star}$  Load and line regulation are specified at constant junction temperature. Change in  $V_0$  due to heating effects must be taken into account separately. Pulse testing with low duty is used



# LM337 (KA337) ADJUSTABLE VOLTAGE REGULATOR (NEGATIVE)

# **TYPICAL APPLICATIONS**

Fig. 1 Programmable Regulator



inches from power supply filter.

A  $1.0\mu F$  solid tantalum or  $10\mu F$  aluminum electrolytic is recommended. Co is necessary for stability. A  $1.0\mu F$  solid tantalum or  $10\mu F$  aluminum electrolytic

 $V_0 = -1.25V (1 + R_2/R_1)$ 

\* Ci is required if regulator is located more then 4



The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## **PRODUCT STATUS DEFINITIONS**

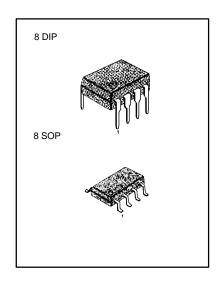
Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

## **DUAL OPERATIONAL AMPLIFER**

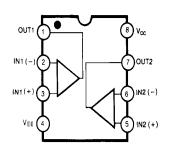
The LF353 is a JFET input operational amplifier with an internally compensated input offset voltage. The JFET input device provides with bandwidth, low input bias currents and offset currents.

# **FEATURES**

- Internally trimmed offset voltage: 10mV
- Low input bias current: 50pA
- Wide gain bandwidth: 4MHz
- High slew rate: 13V/μs
- High Input impedance:  $10^{12}\Omega$



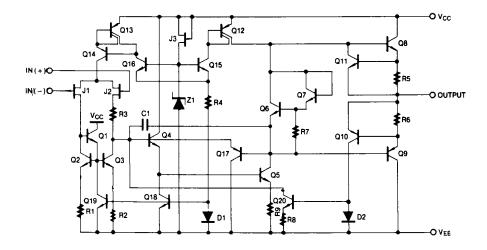
# **BLOCK DIAGRAM**



## **ORDERING IN FORMATION**

Device	Package	Operating Temperature
LF353N	8 DIP	
LF353M	8 SOP	0 ~ + 70°C
LF353S	9 SIP	

# SCHEMATIC DIAGRAM (One Section Only)





# **ABSOLUTE MAXIMUM RATINGS**

Characteristics	Symbol	Value	Unit
Power Supply Voltage	Vcc	±18	V
Differential Input Voltage	V <sub>I(DIFF)</sub>	30	V
Input Voltage Range	VI	±15	V
Output Short Circuit Duration		Continuous	
Power Dissipation	P <sub>D</sub>	500	mW
Operating Temperature Range	T <sub>OPR</sub>	0 ~ +70	°C
Storage Temperature Range	T <sub>STG</sub>	-65 ~ +150	°C

# **ELECTRICAL CHARACTERISTICS**

(V<sub>CC</sub> =+15V, V<sub>EE</sub>= -15V,  $T_A$ =25 °C, unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Тур	Max	Unit
Innuit Offeet Veltege	V <sub>IO</sub>	Rs=10KΩ			5.0	10	\/
Input Offset Voltage	VIO		$0 ^{\circ}\text{C} \leq T_{A} \leq +70 ^{\circ}\text{C}$				mV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	$R_S=10K\Omega$	$0 ^{\circ}\text{C} \leq T_{A} \leq +70 ^{\circ}\text{C}$		10		μV/°C
Input Offset Current	IIO				25	100	pА
input onset ourient	IIO		$0 {}^{\circ}\text{C} \leq T_{A} \leq +70 {}^{\circ}\text{C}$			4	nA
Input Bias Current	1				50	200	pА
Input Bias Current	I <sub>BIAS</sub>		$0 {}^{\circ}\text{C} \leq T_{A} \leq +70 {}^{\circ}\text{C}$			8	nA
Input Resistance	R <sub>I</sub>				10 <sup>12</sup>		Ω
		$V_{O(P-P)} = \pm 0V$		25	100		V/mV
Large Signal Voltage Gain	G∨	$R_L = 2K\Omega$	$0 ^{\circ}\text{C} \leq T_{A} \leq +70 ^{\circ}\text{C}$	15			V/IIIV
Output Voltage Swing	V <sub>O(P.P)</sub>	$R_L = 10K\Omega$		±12	±13.5		V
Input Voltage Range	$V_{I(R)}$			±11	±15/-12		V
Common Mode Rejection Ratio	CMRR	R <sub>S</sub> ≥10KΩ		70	100		dB
Power Supply Rejection Ratio	PSRR	R <sub>S</sub> ≥10KΩ		70	100		dB
Power Supply Current	Icc				3.6	6.5	mA
Slew Rate	SR	G <sub>V</sub> = 1			13		V/µs
Gain-Bandwidth Product	GBM				4		MHz
Channel Seperation	cs	f = 1Hz ~ 20 (Input refere		120	120		dB
Equivalent Input Noise Voltage	V <sub>NI</sub>	$R_S = 100\Omega$ f = 1KHz		16	16		nV/√Hz
Equivalent Input Noise Current	I <sub>NI</sub>	f = 1KHz		0.01	0.01		pA/√ <sup>Hz</sup>



The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

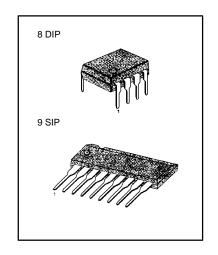
## **PRODUCT STATUS DEFINITIONS**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

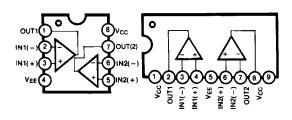
# **DUAL JFET INPUT OPERATIONAL**

# **FEATURES**

- Low supply current: 400pA MAX
- Low input bias Current: 50pA MAX
- Low input offset voltage: 1mV MAX
  High slew rate: 1V/µs
  High gain bandwidth: 1MHz



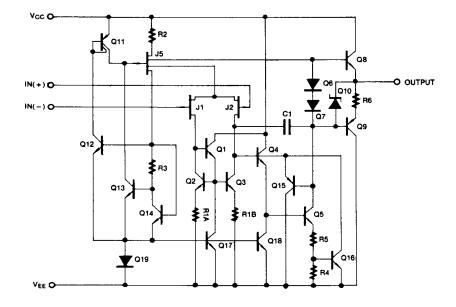
# **BLOCK DIAGRAM**



# **ORDERING INFORMATION**

Device	Package	Operating Temperature			
LM442N LM442AN	8 DIP				
LM442S LM442AS	9 SIP	0 ~ +70°C			

# SCHEMATIC DIAGRAM (One Section Only)





# **ABSOLUTE MAXIMUM RATINGS**

Characteristics	Symbol	Value	Unit
Power Supply Voltage LM442	V	±18	V
LM442A	V <sub>cc</sub>	±20	V
Differential Input Voltage	$V_{I(DIFF)}$	30	V
Input Voltage range	$V_{l}$	±15	V
Output Short Circuit Duration		Continuous	
Power Dissipation	P <sub>D</sub>	670	mW
Operating Temperature Range LM442/A	T <sub>OPR</sub>	0 ~ + 70	°C
Storage Temperature Range	T <sub>STG</sub>	-65 ~ <b>+</b> 150	°C

# **ELECTRICAL CHARACTERISTICS**

(T<sub>A</sub>=25  $^{\circ}$ C, unless otherwise specified)

<b>A</b> 1 1.4		Symbol Test Conditions		LM442A			LM442			Init
Characteristic	Symbol			Min	Тур	Max	Min	Тур	Max	mit
Input Offset Voltage		$R_S = 10K\Omega$			0.5	1.0		1.0	5.0	mV
Indut Offset Voltage	V <sub>IO</sub>	_	Note 1						7.5	
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	$R_S = 10K\Omega$			7	10		7		μV/°C
Input Offset Current	I <sub>IO</sub>				5	25		5	50	ρA
input Onset Guitent	-10		Note 1			15			15	ρ, ,
Large Signal Voltage Gain	I <sub>BIAS</sub>				10	50		10	100	pA
Large Oignar Voltage Cam	•DIAS		Note 1			30			30	ρ, ,
Large Signal Voltage Gain	Gv	$R_L = 10K\Omega$		50	200		25	200		V/mV
Largo Cignar Voltago Cam	ΟV	$V_{O(P.P)} = \pm 0V$	Note 1	25	200		15	200		
Output Voltage Swing	$V_{O(P-P)}$	$R_S = 10K\Omega$		±17	±18		±12	±13		V
Input Voltage Range	$V_{I(R)}$			±16	+18 -17		±11	+15 -12		V
Common-Mode Rejection Ratio	CMRR	R <sub>S</sub> ≤10KΩ		80	100		70	95		dB
Power Supply Rejection Ratio	PSRR	R <sub>S</sub> ≤10KΩ		80	100		70	90		dB
Input Resistance	Rı				10 <sup>12</sup>		10 <sup>12</sup>			Ω
Supply Current	Icc				300	400		400	500	μΑ
Slew Rate	SR			0.8	1		0.6	1		V/μS
Gain Bandwidth Product				0.8	1		0.6	1		MHz
Channel Separation	CS	f = 1Hz-20KHz (input reference			120			120		dB
Equivalent Input Noise Voltage	V <sub>NI</sub>	$R_S = 100\Omega$ f = 1KHz			35			35		n <u>V/</u> √Hz
Equivalent Input Noise Current	I <sub>NI</sub>	f = 1KHz			0.01			0.01		p <u>A /</u> √ Hz

NOTE 1. LM442/A :  $0 \le T_A \le +70 \,^{\circ}\text{C}$ 



The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## **PRODUCT STATUS DEFINITIONS**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

## **SINGLE TIMER**

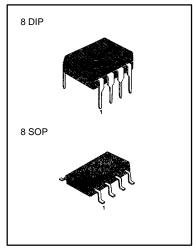
The LM555/l is a highly stable controller capable of producing accurate timing pulses. With monostable operation, the time delay is controlled by one external and one capacitor. With astable operation, the frequency and duty cycle are accurately controlled with two external resistors and one capacitor.

# **FEATURES**

- High Current Drive Capability (= 200mA)
- Adjustable Duty Cycle
- Temperature Stability of 0.005%/°C
- $\bullet$  Timing From  $\mu Sec$  To Hours
- Turn Off Time Less Than 2μSec

# **APPLICATIONS**

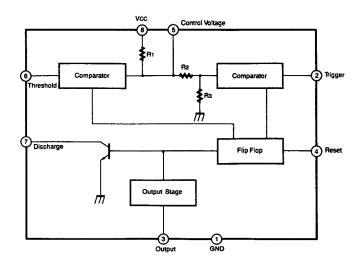
- Precision Timing
- Pulse Generation
- Time Delay Generation
- Sequential Timing



## **ORDERING INFORMATION**

Device	Package	Operating Temperature
LM555CN	8 DIP	0 ~ +70°C
LM555CM	8 SOP	0 ~ +70°C
LM555CIN	8 DIP	40 .95°C
LM555CIM	8 SOP	-40 ~ +85°C

# **BLOCK DIAGRAM**





### **SINGLE TIMER**

### ABSOLUTE MAXIMUM RATINGS $(T_A = 25^{\circ}C)$

Characteristic	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	16	V
Lead Temperature (soldering 10sec)	T <sub>LEAD</sub>	300	°C
Power Dissipation	$P_D$	600	mW
Operating Temperature Range LM555C LM555CI	T <sub>OPR</sub>	0 ~ + 70 - 40 ~ + 85	°C °C
Storage Temperature Range	T <sub>STG</sub>	- 65 ~ + 150	°C

 $\begin{tabular}{ll} \textbf{ELECTRICAL CHARACTERISTICS} \\ (T_A = 25 ^{\circ}C, \, V_{CC} = 5 \sim 15 V, \, unless \, otherwise \, specified) \\ \end{tabular}$ 

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
Supply Voltage	V <sub>CC</sub>		4.5		16	V
Supply Current		V <sub>CC</sub> = 5V, R <sub>L</sub> = ∞		3	6	mA
*1(low stable)	Icc	V <sub>CC</sub> = 15V, R <sub>L</sub> = ∞		7.5	15	mA
*Timing Error						
(Monostable)						
<sup>2</sup> Initial Accuracy	ACCUR	$R_A = 1K\Omega$ to		1.0	3.0	%
Drift with Temperature	$\Delta t/\Delta T$	100ΚΩ		50		ppm/°C
Drift with Supply Voltage	$\Delta t/\Delta V_{CC}$	$C = 0.1 \mu F$		0.1	0.5	%/V
*Timing Error						
(astable)		$R_A = 1K\Omega$ to $100K\Omega$				
<sup>2</sup> Intial Accuracy	ACCUR	$C = 0.1 \mu F$		2.25		%
Drift with Temperature	$\Delta t/\Delta T$			150		ppm/°C
Drift with Supply Voltage	$\Delta t/\Delta V_{CC}$			0.3		%/V
Control Voltage	Vc	V <sub>CC</sub> = 15V	9.0	10.0	11.0	V
Control voltage	V.C	$V_{CC} = 5V$	2.6	3.33	4.0	V
Threshold Voltage	$V_{TH}$	V <sub>CC</sub> = 15 V		10.0		V
Threshold Voltage	VIII	$V_{CC} = 5V$		3.33		V
*3Threshold Current	I <sub>TH</sub>			0.1	0.25	μΑ
Trigger Voltage	$V_{TR}$	$V_{CC} = 5V$	1.1	1.67	2.2	V
Trigger Voltage	$V_{TR}$	V <sub>CC</sub> = 15V	4.5	5	5.6	V
Trigger Current	I <sub>TR</sub>	$V_{TR} = 0V$		0.01	2.0	μΑ
Reset Voltage	$V_{RST}$		0.4	0.7	1.0	V
Reset Current	I <sub>RST</sub>			0.1	0.4	mA



#### **ELECTRICAL CHARACTERISTICS**

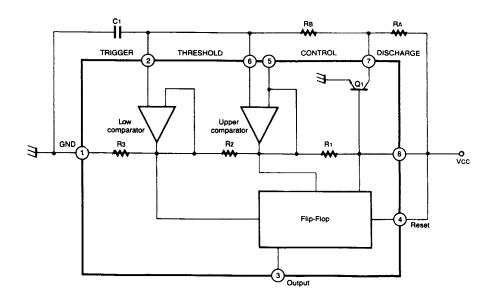
 $(T_A = 25^{\circ}C, V_{CC} = 5 \sim 15V, \text{ unless otherwise specified})$ 

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
		V <sub>CC</sub> = 15V				
		I <sub>SINK</sub> = 10mA		0.06	0.25	V
Low Output Voltage	$V_{OL}$	I <sub>SINK</sub> = 50mA		0.3	0.75	V
		$V_{CC} = 5V$				
		I <sub>SINK</sub> = 5mA		0.05	0.35	V
		V <sub>CC</sub> = 15V				
		I <sub>SOURCE</sub> = 200mA		12.5		V
High Output Voltage	V <sub>OH</sub>	I <sub>SOURCE</sub> = 100mA	12.75	13.3		V
		$V_{CC} = 5V$				
		I <sub>SOURCE</sub> = 100mA	2.75	3.3		V
Rise Time of Output	t <sub>R</sub>			100		ns
Fall Time of Output	t <sub>F</sub>			100		ns
Discharge Leakage Current	$I_{LKG}$			20	100	nA

#### Notes:

- 1. Supply current when output is high is typically 1mA less at  $V_{CC}$  = 5V 2. Tested at  $V_{CC}$  = 5.0V and  $V_{CC}$  = 15V
- 3. This will determine maximum value of  $R_A + R_B$  for 15V operation, the max. total  $R = 20M\Omega$ , and for 5V operation the max. total R =  $6.7M\Omega$

#### **APPLICATION CIRCUIT**





#### **APPLICATION NOTE**

The application circuit shows a stable mode. Pin 6 (threshold) is tied to Pin 2 (trigger) and Pin 4 (reset) is tied to  $\rm V_{CC}$  (Pin 8).

The external capacitor C<sub>1</sub> of Pin 6 and Pin 2 charges through R<sub>A</sub>, R<sub>B</sub> and discharges through R<sub>B</sub> only.

In the internal circuit of the LM555 one input of the upper comparator is the  $2/3 \text{ V}_{CC}$  (\*R<sub>1</sub> =R<sub>2</sub>=R<sub>3</sub>, another input if it If it is connected Pin 6.

As soon as charging C<sub>1</sub> is higher than 2/3 Vcc, discharge transistor Q<sub>1</sub> turns on and C<sub>1</sub> discharges to collector of transistor Q<sub>1</sub>.

Therefore, the flip-flop circuit is reset and output is low.

One input of lower comparator is the 1/3 V<sub>CC</sub>, discharge transistor Q<sub>1</sub> turn off and C<sub>1</sub> charges through R<sub>A</sub> and R<sub>B</sub>. Therefore, the flip-flop circuit is set and output is high.

So to say, when  $C_1$  charges through  $R_A$  and  $R_1$  output is high and when  $C_1$  discharges through  $R_B$  output is low. The charge time (output is high)  $T_1$  is 0.693 ( $R_A+R_B$ )  $C_1$  and the discharge time (output is low)  $T_2$  is 0.693 ( $R_B$   $C_1$ ).

$$(I_n \frac{V_{CC}-1/3}{V_{CC}-2/3}V_{CC})$$

Thus the total period time T is given by

 $T=T_1+T_2=0.693~(R_A+2R_B)~C_1.$  Then the frequency of astable mode is given by

$$f = = \frac{1}{T} - \frac{1.44}{(R_A + 2R_B)C_1}$$

The duty cycle is given by

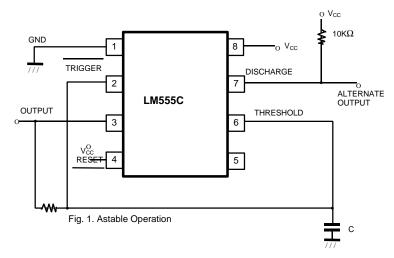
$$D.C = \frac{T_{e}}{T} \frac{R_{B}}{R_{A} + 2R_{B}}$$

If you make use of the LM556 you can make two astable modes.



#### **Astable Operation**

The LM555 can free run as a mulitivibrator by triggering itself; refer to Fig.2. The output can swing from  $V_{DD}$  to GND and have 50 duty cycle square wave. Less than 1% frequency deviation can be observed, over a voltage range of 2 to 5V. f-1/1.4RC



#### **Monostable Operation**

The LM555 can be used as a one-short, i.e. monostable multivibrator. Initially, because the inside discharge transistor is on state, external timing capacitor is held to GND potential. Upon application of a negative TRIGGER pulse pin 2, the intern discharge transistor is off state and the voltage across the capacitor increases with time constant T =  $R_A$ C and OUTPUT goes to high state. When the voltage across the capacitor equals  $2/3V_{CC}$  the inner comparator is reset by THRESHOLD input and the discharge transistor goes to on state, which in turn discharges the capacitor rapidly and drives the OUTPUT to its low state.

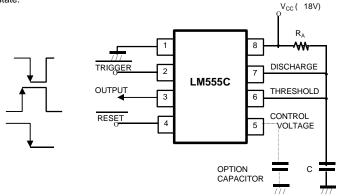


Fig. 2. Monostable Operation



#### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

#### **PRODUCT STATUS DEFINITIONS**

#### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

#### **DUAL TIMER**

The LM556/I series dual monolithic timing circuits are a highly stable controller capable of producing accurate time delays or oscillation. The LM556 is a dual LM555. Timing is provided an external resistor and capacitor for each timing function.

The two timers operate independently of each other, sharing only  $V_{\text{CC}}$  and ground.

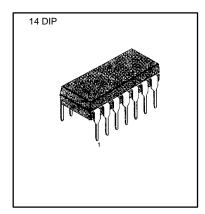
The circuits may be triggered and reset on falling wave forms. The output structures may sink or source 200mA.

#### **FEATURES**

- Replaces Two LM555C Timers
- Operates in Both Astable and Monostable Modes
  High Output Current
- TTL Compatible
- Timing From Microsecond to Hours
- Adjustable Duty Cycle
- Temperature Stability Of 0.005% Per °C

#### **APPLICATIONS**

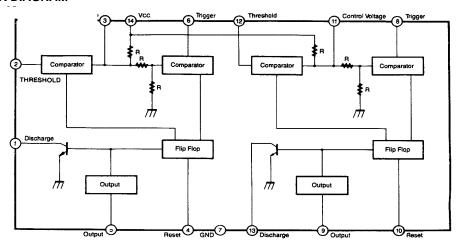
- Precision Timing
- Pulse Shaping
- Pulse Width Modulation
- Frequency Division
- Traffic Light Control
- Sequential Timing
- Pulse Generator
- Time Delay Generator
- Touch Tone Encoder
- Tone Burst Generator



#### **ORDERING INFORMATION**

Device	Package	Operating Temperature
LM556CN	14 DIP	0 ~ + 70°C
LM556ICN	14 DIP	-40 ~ + 85°C

#### **BLOCK DIAGRAM**





### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V <sub>cc</sub>	16	V
Lead Temperature (soldering 10sec)	T <sub>LEAD</sub>	300	°C
Power Dissipation	P <sub>D</sub>	600	mW
Operating Temperature Range LM556 LM556I	T <sub>OPR</sub>	0 ~ + 70 - 40 ~ + 85	°C °C
Storage Temperature Range	T <sub>STG</sub>	- 65 ~ + 150	°C

### **ELECTRICAL CHARACTERISTICS**

( $T_A = 25^{\circ}C$ ,  $V_{CC} = 5 \sim 15V$ , unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
Supply Voltage	V <sub>CC</sub>		4.5		16	V
*1 Supply Current (two timers)	I <sub>cc</sub>	$V_{CC} = 5V, R_L = \infty$		5	12	mA
(low state)	icc	V <sub>CC</sub> = 15V, R <sub>L</sub> = ∞		16	30	mA
*2 Timing Error (monostable)		$R_A = 2k\Omega$ to $100k\Omega$				
Initial Accuracy	ACCUR	$C = 0.1 \mu F$		0.75		%
Drift with Temperature	$\Delta t/\Delta T$	T = 1.1RC		50		ppm/°C
Drift with Supply Voltage	$\Delta t/\Delta V_{CC}$			0.1		%/V
Control Voltage	V <sub>C</sub>	V <sub>CC</sub> = 15V	9.0	10.0	11.0	V
Control voltage	V <sub>C</sub>	$V_{CC} = 5V$	2.6	3.33	4.0	V
Threshold Voltage	$V_{TH}$	$V_{CC} = 15V$	8.8	10.0	11.2	V
Threshold voltage	VIH	$V_{CC} = 5V$	2.4	3.33	4.2	V
*3 Threshold Voltage	I <sub>TH</sub>			30	250	nA
Trigger Voltage	$V_{TR}$	V <sub>CC</sub> = 15V	4.5	5.0	5.6	V
Trigger Voltage		$V_{CC} = 5V$	1.1	1.6	2.2	V
Trigger Current	I <sub>TR</sub>	$V_{TH} = 0V$		0.01	2.0	μΑ
*5 Reset Voltage	V <sub>RST</sub>		0.4	0.6	1.0	V
Reset Current	I <sub>RST</sub>			0.03	0.6	mA
		V <sub>CC</sub> = 15V				
		I <sub>SINK</sub> = 10mA		0.1	0.25	V
		I <sub>SINK</sub> = 50mA		0.4	0.75	V
Low Output Voltage	$V_{OL}$	I <sub>SINK</sub> = 100mA		2.0	3.2	V
		I <sub>SINK</sub> = 200mA		2.5		V
		V <sub>CC</sub> = 5V				
		I <sub>SINK</sub> = 8mA		0.25	0.35	V
		$I_{SINK} = 5mA$		0.15	0.25	V



#### **ELECTRICAL CHARACTERISTICS**

 $(T_A = 25^{\circ}C, V_{CC} = 5 \sim 15V, \text{ unless otherwise specified})$ 

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
		V <sub>CC</sub> = 15V				
		I <sub>SOURCE</sub> = 200mA		12.5		V
High Output Voltage	V <sub>OH</sub>	I <sub>SOURCE</sub> = 100mA	12.75	13.3		V
		V <sub>CC</sub> = 5V				
		I <sub>SOURCE</sub> = 100mA	2.75	3.3		V
Rise Time of Output	t <sub>R</sub>			100	300	ns
Fall Time of Output	t <sub>F</sub>			100	300	ns
Discharge Leakage Current	$I_{LKG}$			10	100	nA
*4 Matching Characteristics						
Initial Accuracy	ACCUR			1.0	2.0	%
Drift with Temperature	$\Delta t/\Delta T$			10		ppm/°C
Drfit with Supply Voltage	$\Delta t/\Delta V_{CC}$			0.2	0.5	%/V
*2 Timing Error (astable)		$R_A, R_B = 1k\Omega$ to $100k\Omega$				
Initial Accuracy	ACCUR	C = 0.1μF		2.25		%
Drift with Temperature	$\Delta t/\Delta T$	V <sub>CC</sub> = 15V		150		ppm/°C
Drift with Supply Voltage				0.3		%/V

#### Notes:

- \*1. Supply current when output is high is typically 1.0mA less at  $V_{\text{CC}} = 5V$
- \*2. Tested at  $V_{CC}$  = 5V and  $V_{CC}$  = 15V
- \*3. This will determine the maximum value of  $R_A+R_B$  for 15V operation. The maximum total  $R=20M\Omega$ , and for 5V operation the maximum total  $R=6.6M\Omega$ .
- \*4. Matching characteristics refer to the difference between performance characteristics of each timer section in the monostable mode.
- \*5. As reset voltage lowers, timing is inhibited and then the output goes low.



#### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

#### **PRODUCT STATUS DEFINITIONS**

#### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

#### **HIGH SPEED VOLTAGE COMPARATOR**

The LM710/I is a high speed voltage comparator intended for use as an accurate, low-level digital level sensor or as a replacement for operational amplifiers in comparator applications where speed is of prime

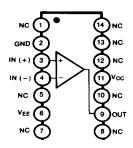
The output of the comparator is compatible with all integrated logic

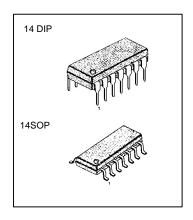
The LM710/I is useful as pulse height discriminators. a variable threshold Schmitt trigger, voltage comparator in high-speed A/D converters, a memory sense amplifier or a high noise immunity line receiver.

#### **FEATURES**

- Low offset voltage: 5mVHigh gain: 1000 V/V
- High speed: 40ns Typ

#### **BLOCK DIAGRAM**

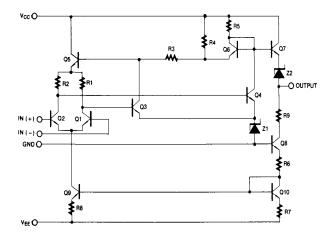




#### **ORDERING INFORMATION**

Device	Package	Operating Temperature
LM710N	14 DIP	0 ~ 70°C
LM710M	14 SOP	
LM710IN	14 DIP	-25 ~ 85°C
LM710IM	14 SOP	

#### **SCHEMATIC DIAGRM**





### **ABSOLUTE MAXIMUM RATINGS**

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	V <sub>cc</sub>	+14	V
Negative Supply Voltage	$V_{EE}$	-7	V
Peak Output Current	$I_{PK}$	10	mA
Output Short Circuit Duration		10	Sec
Differential Input Voltage	$V_{I(DIFF)}$	5	V
Input Voltage	$V_{I}$	± 7	V
Power Dissipation	$P_D$	500	mW
Operating Temperature Range LM710	T <sub>STG</sub>	0 ~ + 70	°C
LM710I	' STG	- 25 ~ + 85	°C
Storage Temperature Range	$T_{STG}$	- 65 ~ <b>+</b> 150	°C

### **ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> = +12V, V<sub>EE</sub>= -6V, T = 25°C, unless otherwise specified)

Characteristics	Symbol	Test Co	onditions		LM710I		LM710			UNIT
				Min	Тур	Max	Min	Тур	Max	
Input Offset voltage	V <sub>IO</sub>	R <sub>S</sub> ≤200Ω,	Note1		0.6	2.0		1.6	5.0	mV
			Note 2			3.0			6.5	
Input Offset Current	I <sub>IO</sub>	NOTE 1			0.75	3.0		1.8	5.0	nA
(Note 1)			Note 2		1.8	7.0			7.5	
Input Bias Current	I <sub>BIAS</sub>				5.0	20		7.0	25	nA
			Note 2		27	45		25	40	
Large Signal Voltage Gain	$G_v$			1250	1800		1000	1700		V/V
			Note 2							
Input Voltage Range	$V_{I(R)}$	$V_{CC} = -7V$		± 5.0			± 5.0			V
Common Mode Rejection Ratio	CMRR	R <sub>S</sub> ≤200Ω, N	NOTE 2	80	95		70	94		dB
Differential Input Voltage Range	$V_{ID(R)}$			± 5.0			± 5.0			٧
Positive Output Level	$V_{O(H)}$	$0 \le I_0 \le 5mA$	, V <sub>I</sub> ≥5mV	2.5	2.9	4.0	2.5	2.9	4.0	V
Negative Output Level	$V_{O(L)}$	V <sub>I</sub> ≥5mV		-1.0	-0.5	0	-1.0	-0.5	0	V
Output Sink Current	I <sub>SINK</sub>	V <sub>O(P)</sub> =0V, ∖	/ <sub>I</sub> ≥5mV	2.0	2.2		1.6	2.2		mA
Positive Supply Current	I <sub>cc</sub>	$V_{O(P)} \le 0V$			4.7	9.0		4.7	9.0	mA
Negative Supply Current	I <sub>EE</sub>	$V_{O(P)} = 0V$	$V_I = 5mV$		4.0	7.0		4.0	7.0	mA
Power Consumption	$P_D$	$V_{O(P)} = 0V,$	V <sub>I</sub> =10mV		80	150			150	mV
Response Time	t <sub>RES</sub>	(Note 3)			40			40		ns

Note 1. The input offset voltage and input offset current are specified for a logic threshold voltage as follows:

For 7101, 1.65V at -25°C, 1.4V at +25°C, 1.15V at +85°C. For 710, 1.5V at 0°C, 1.4V at +25°C, 1.2V at +70°C.

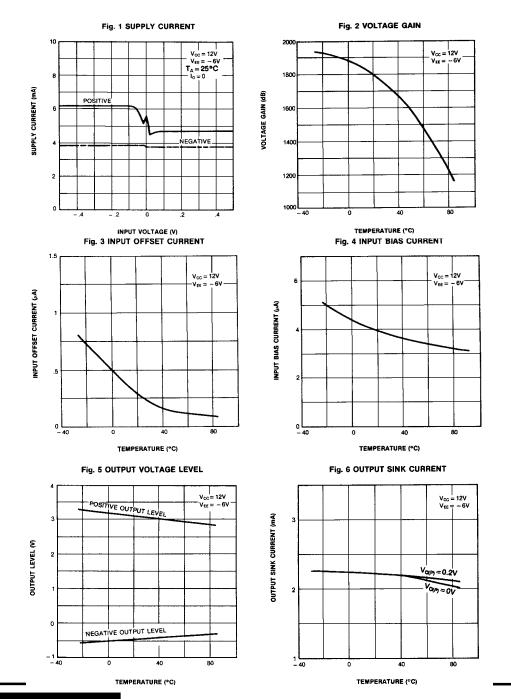
Note 2. LM710: 0≤ TA≤ +70°C

LM710I:-25≤ TA≤ +85°C

Note 3. The response time specified is a 100mV input step with 5mV overdrive (LM710).



#### TYPICAL PERFORMANCE CHARACTERISTICS





#### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

#### **PRODUCT STATUS DEFINITIONS**

#### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

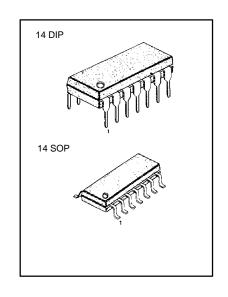
# DUAL HIGH-SPEED DIFFERENT COMPARATOR

The LM711/I consists of two voltage comparators with the separate differential inputs, a common output and provision for strobing each side independently. The device features high accuracy, fast response, low offset voltage, a large input voltage range, low power consumption and compatibility with practically all integrated logic forms.

The LM711/I can be used as a sense amplifier for memories, and a dual comparator with OR'ed outputs is required, such as a double-ended limit detector.

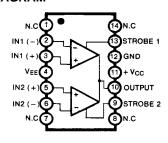
#### **FEATURES**

- Fast response time: 40ns (Typ)
- Output compatible with most TTL circuits
- Independent strobing of each comparator
- Low offset voltage



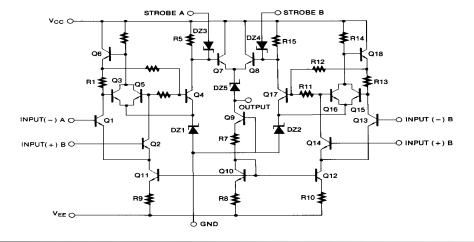
#### **ORDERING INFORMATION**

#### **BLOCK DIAGRAM**



Device	Package	Operating Temperature
LM711N	14 DIP	0 ~ + 70°C
LM711M	14 SOP	0~+70°C
LM711IN	14 DIP	-25 ~ + 85°C
LM711IM	14 SOP	-20 ~ + 60°C

#### **SCHEMATIC DIAGRAM**





#### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C)

Characteristic	Symbol	Value	Unit
Positive Supply Voltage	V <sub>CC</sub>	+14	V
Negative Supply Voltage	V <sub>EE</sub>	-7	V
Differential Input Voltage	$V_{I(DIFF)}$	5	V
Input Voltage	Vı	±7	V
Storbe Voltage	V <sub>STR</sub>	0 ~ 6	V
Peak Output Current	I <sub>O(P)</sub>	50	mA
Continuous Total Power Dissipation	$P_{D}$	500	mW
Operating Temperature Range LM711		0 ~ + 70	
LM711I	T <sub>OPR</sub>	-65 ~ <b>+</b> 150	°C
Storage Temperature Range	T <sub>STG</sub>	-25 ~ + 85	°C

#### **ELECTRICAL CHARACTERISTICS**

( $V_{CC}$  = +12V,  $V_{EE}$  = -6V,  $T_A$ =25°C, unless otherwise specified)

Characteristic	Cumbal	Test Conditions			LM711I			LM711		Unit
Characteristic	Symbol	rest Cor	rest Conditions		Тур	Max	Min	Тур	Max	Unit
Input Offset Voltage	V <sub>IO</sub>	R <sub>S</sub> ≤200Ω, V <sub>0</sub>	он =0V		1.0	3.5		1.0	5.0	mV
input Onset voltage	VIO	V <sub>O(P)</sub> =1.4V	Note 2			4.5			6.0	1117
Input Offset Current	I <sub>IO</sub>	V <sub>O(P)</sub> =1.4V			0.5	10.0		0.5	15	μΑ
(Note 1)	-10		Note 2			20			25	F** .
Input Bias Current	I <sub>BIAS</sub>				25	75		25	100	μΑ
input bias current	·BIAG		Note 2			150			150	F** .
Large Signal Voltage Gain	G√			750	1500		700	1500		V/V
Large Oighai Voltage Calif	Οv		Note 2	500			500			V/V
Input Voltage Range	$V_{I(R)}$	$V_{EE} = -7.0V$		±5.0			±5.0			V
Differential Input Voltage Range	$V_{ID(R)}$			±5.0			±5.0			V
Output Resistance	Ro				200			200		Ω
Output Voltage (High)	V <sub>O(H)</sub>	V <sub>I</sub> ≥10mV			4.5	5.0		4.5	5.0	V
Output Voltage (Low)	V <sub>O(L)</sub>	V <sub>I</sub> ≤10mV		-1.0		0	-1.0	-0.5	0	V
Loaded Output High Level	V <sub>OH</sub>	V <sub>I</sub> ≥5mV, I <sub>O</sub> =	5mA	2.5	3.5		2.5	3.5		mA
Strobed Output Level	$V_{STR}$	V <sub>STROBE</sub> ≥3V		-1.0		0	-1.0		0	V
Output Sink Current	I <sub>SINK</sub>	V <sub>I</sub> ≥10mV, V <sub>O</sub>	<sub>(P)</sub> ≥0V	0.5	0.8		0.5	0.8		mA
Positive Supply Current	Icc	$V_{O(P)} = 0V, V_I$	= 10mV		8.6			8.6		mA
Negative Supply Current	I <sub>EE</sub>	$V_{O(P)} = 0V, V_I$	=5mV		3.9			3.9		mA
Strobe Current	I <sub>STR</sub>	V <sub>STROBE</sub> = 10	0mV		1.2	2.5		1.2	2.5	mA
Power Consumption	P <sub>D</sub>	V <sub>O(P)</sub> =0V, V <sub>I</sub> 2	≥10mV		130	200		130	230	mW
Response Time	t <sub>RES</sub>	(NOTE 1)	•		40			40		ns
Strobe Release Time	T <sub>RE</sub>		•		12			12		ns

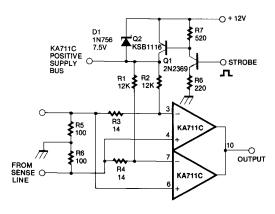
Note: 1. The response time specified is for a 100mV input step with 10mV overdrive

- 2. LM711: 0≤T<sub>A</sub>≤ +70°C
- LM711: -25≤T<sub>A</sub>≤ +85°C
   The input offset voltage and input offset current are specified for a logic threshold voltage of 711I, 1.65V at -25°C, 1.4V at +25°C, 1.15V at +85°C, for 711, 1.5V at 0°C, 1.4V at +25°C, 1.2V at +70°C.



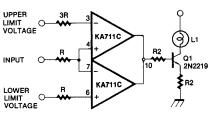
#### **TYPICAL APPLICATIONS**

\*Fig. 1 Sense Amplifier With Supply Strobing for Reduced Power Consumption\*



\* Standby dissipation is about 40mW

Fig. 2 Double-Ended Limit Detactor With Lamp Driver





#### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

#### **PRODUCT STATUS DEFINITIONS**

#### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

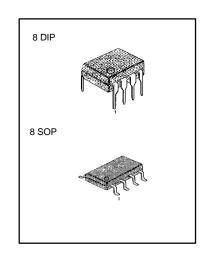
#### SINGLE OPERATIONAL AMPLIFIERS

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. It is intended for a wide range of analog applications.

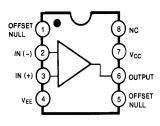
The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier, and general feedback applications.

#### **FEATURES**

- Short circuit protection
- Excellent temperature stability
- Internal frequency compensation
- High Input voltage range
- Null of offset



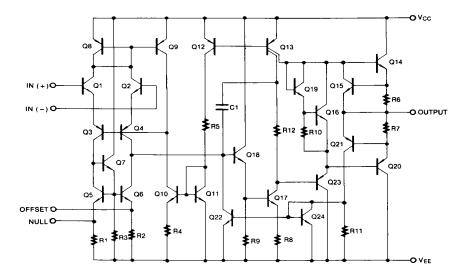
#### **BLOCK DIAGRAM**



#### **ORDERING INFORMATION**

Device	Package	Operating Temperature
LM741N	8 DIP	
LM741EN	0.511	0 ~ + 70°C
LM741M	8 SOP	0~+70 C
LM741EM	0 001	
LM741IN	8 DIP	
LM741EIN	O DII	40 0500
LM741IM	8 SOP	-40 ~ +85 °C
LM741EIM	0 30F	

#### **SCHEMATIC DIAGRAM**





### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25 °C)

Characteristic	Symbol	LM741	LM741E	LM741I	Unit
Supply Voltage	V <sub>CC</sub>	±18	±22	±18	V
Differential Input Voltage	$V_{I(DIFF)}$	30	30	30	V
Input Voltage	$V_{I}$	±15	±15	±15	V
Output Short Circuit Duration		Indefinite	Indefinite	Indefinite	
Power Dissipation	$P_D$	500	500	500	mW
Operating Temperature Range	$T_{OPR}$	0 ~ + 70	0 ~ + 70	-40 ~ + 85	°C
Storage Temperature Range	$T_{STG}$	-65 ~ + 150	-65 ~ + 150	-65 ~ <b>+</b> 150	°C

**ELECTRICAL CHARACTERISTICS** ( $V_{CC}$  = 15V,  $V_{EE}$  = -15V.  $T_A$  = 25 °C, unless otherwise specified)

Characteristic	Symbol	Test Conditions			LM741	=	LM	741/LM	741I	I I m i 4
Characteristic	Symbol	Test Cor	iditions	Min	Тур	Max	Min	Тур	Max	Unit
	V <sub>IO</sub>	R <sub>S</sub> ≤10KΩ						2.0	6.0	
Input Offset Voltage	VIO	R <sub>S</sub> ≤50Ω			8.0	3.0				mV
Input Offset Voltage	V <sub>IO(R)</sub>	$V_{CC} = \pm 20V$		±10				±15		mV
Adjustment Range	- ( ,	00								
Input Offset Current	I <sub>IO</sub>				3.0	30		20	200	nA
Input Bias Current	I <sub>BIAS</sub>				30	80		80	500	nA
Input Resistance	$R_{l}$	V <sub>CC</sub> =±20V		1.0	6.0		0.3	2.0		$M\Omega$
Input Voltage Range	$V_{I(R)}$			±12	±13		±12	±13		V
			V <sub>CC</sub> =±20V,							
	G <sub>V</sub>	R <sub>L</sub> ≥2KΩ	V <sub>O(P.P)</sub> =±15V	50						
Large Signal Voltage Gain			V <sub>CC</sub> =±15V,				20	200	V/mV	
			$V_{O(P.P)} = \pm 10V$				20	200		
Output Short Circuit Current	I <sub>sc</sub>			10	25	35		25		mA
			R <sub>L</sub> ≥10KΩ	±16						
Output Valtage Swing	.,	$V_{CC} = \pm 20V$	R <sub>L</sub> ≥10KΩ	±15						1
Output Voltage Swing	$V_{O(P.P)}$		R <sub>L</sub> ≥10KΩ				±12	±14		V
		$V_{CC} = \pm 15V$	R <sub>L</sub> ≥10KΩ				±10	±13		
		R <sub>S</sub> ≤10KΩ, V <sub>CN</sub>	<sub>M</sub> = ±12V				70	90		
Common Mode Rejection Ratio	CMRR	$R_S \le 50 K\Omega$ , $V_{CM} = \pm 12 V$		80	95					dB
		$V_{CC} = \pm 15V$ to	$V_{CC} = \pm 15V$	86	96					
		R <sub>S</sub> ≤50Ω		30	90					
Power Supply Rejection Ratio	PSRR	$V_{CC} = \pm 15V$ to $V_{CC} = \pm 15V$					77	96		dB
		R <sub>S</sub> ≤10KΩ					''	30		



### **ELECTRICAL CHARACTERISTICS** (Continued)

Charac	teristic	Symbol	Test Conditions		LM741E	Ē	LM7	41/LM	741I	Unit
Citarac	iteristic	Syllibol	rest conditions	Min	Тур	Max	Min	Тур	Max	Oiiit
Transient	Rise Time	t <sub>R</sub>			0.25	0.8		0.3		μs
Response	Overshoot	OS	Unity Gain		6.0	20		10		%
Bandwidth		BW		0.43	1.5					MHz
Slew Rate		SR	Unity Gain	0.3	0.7			0.5		V/μs
Supply Current		Icc	R <sub>L</sub> = ∞Ω					1.5	2.8	mA
		_	$V_{CC} = \pm 20V$		80	150				mW
Power Consum	iption	Pc	$V_{CC} = \pm 15V$					50	85	IIIVV

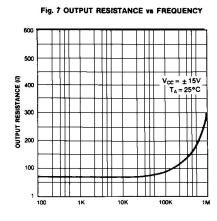
### **ELECTRICAL CHARACTERISTICS**

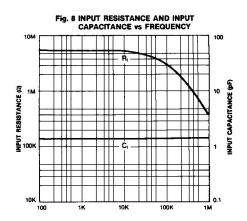
( -40 °C  $\leq$ T<sub>A</sub> $\leq$ 85 °C for the KA7411 °C  $\leq$ T<sub>A</sub> $\leq$ 70 °C for the LM741 and LM741E. V<sub>CC</sub> =  $\pm$ 15V, unless otherwise specified)

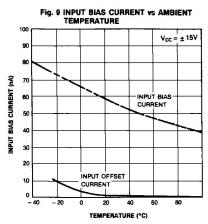
Characteristic	Symbol	Test (	Conditions	ı	LM741	E	LM	741/LN	1741I	Unit
Characteristic	Symbol	rest conditions		Min	Тур	Max	Min	Тур	Max	Unit
Innut Offeet Veltage	R <sub>S</sub> ≤50Ω				4.0				mV	
Input Offset Voltage	V <sub>IO</sub>	R <sub>S</sub> ≤10KΩ							7.5	IIIV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$				15					μV/°C
Input Offset Current	I <sub>IO</sub>					70			300	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$					0.5				nA/°C
Input Bias Current	I <sub>BIAS</sub>					0.21			0.8	μΑ
Input Resistance	R <sub>I</sub>	$V_{CC} = \pm 20V$		0.5						MΩ
Input Voltage Range	$V_{I(R)}$			±12	±13		±12	±13		V
		V <sub>CC</sub> =±20V	R <sub>S</sub> ≥10KΩ	±16						
	.,	V <sub>CC</sub> =±20V	R <sub>S</sub> ≥2KΩ	±15						V
Output Voltage Swing	V <sub>O(P.P)</sub>		R <sub>S</sub> ≥10KΩ				±12	±14		V
		$V_{CC} = \pm 15V$	R <sub>S</sub> ≥2KΩ				±10	±13		
Output Short Circuit Current	I <sub>sc</sub>			10		40	10		40	mA
	OMBB	R <sub>S</sub> ≤10KΩ, V	′ <sub>CM</sub> = ±12V				70	90		9
Common Mode Rejection Ratio	CMRR	R <sub>S</sub> ≤50KΩ, V	′ <sub>CM</sub> = ±12V	80	95					dB
		$V_{CC} = \pm 20V$	R <sub>S</sub> ≤50Ω	86	96					-ID
Power Supply Rejection Ratio	PSRR	to ±5V	R <sub>S</sub> ≤10KΩ				77	96		dB
			$V_{CC} = \pm 20V$ ,	32						
Large Signal Voltage Gain			$V_{O(P-P)} = \pm 15V$							
	G√	R <sub>s</sub> ≥2KΩ	$V_{CC} = \pm 15V$ ,				15			V/mV
	ΟV	NS=ZNS2	$V_{O(P.P)} = \pm 10V$							
			$V_{CC} = \pm 15V$ ,	10						
			$V_{O(P-P)} = \pm 2V$							

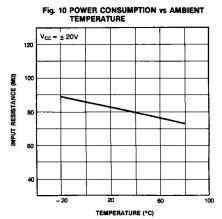


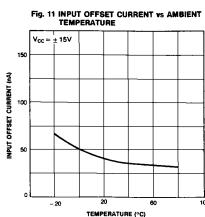
### TYPICAL PERFORMANCE CHARACTERISTICS

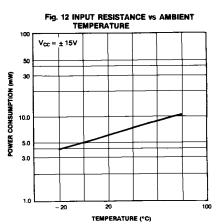




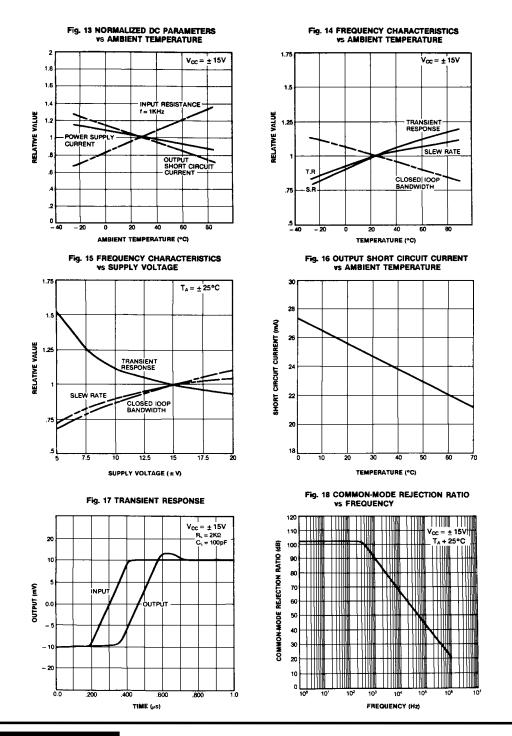




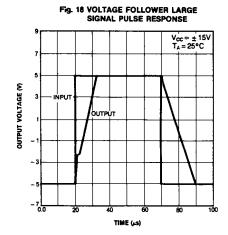


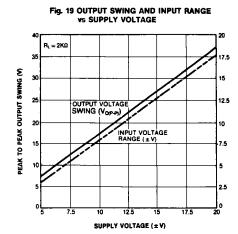


FAIRCHILD SEMICONDUCTOR TM











#### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

#### **PRODUCT STATUS DEFINITIONS**

#### **Definition of Terms**

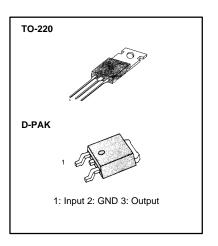
Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

# 3-TERMINAL 1A POSITIVE VOLTAGE REGULATORS

The LM78XX series of three-terminal positive regulators are available in the TO-220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

#### **FEATURES**

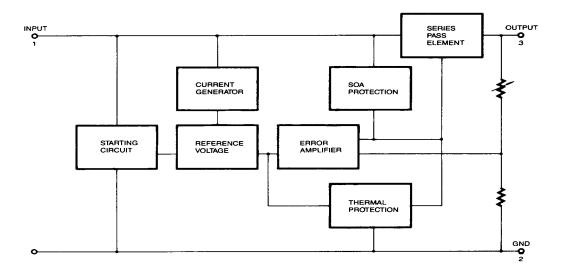
- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 11, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor SOA Protection



#### **ORDERING INFORMATION**

Device	Output Voltage Tolerance	Packag	Operating Temperature
KA78XXCT	± 4%		0 ~ +125 °C
KA78XXAT	± 2%	TO-220	0 ~ +125 °C
KA78XXIT	. 40/		-40 ~ +125 °C
KA78XXR	± 4%		0 1105.00
KA78XXAR	± 2%	D-PAK	0 ~ +125 °C
KA78XXIR	± 4%		-40 ~ +125 °C

#### **BLOCK DIAGRAM**





### **ABSOLUTE MAXIMUM RATINGS** ( $T_A = +25$ °C, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage (for V <sub>O</sub> = 5V to 18V)	Vı	35	V
(for V <sub>O</sub> = 24V)	VI	40	V
Thermal Resistance Junction-Cases	$R_{\theta JC}$	5	°C/W
Thermal Resistance Junction-Air	$R_{\theta JA}$	65	°C/W
Operating Temperature Range KA78XX/A/R/RA KA78XXI/RI	T <sub>OPR</sub>	0 ~ +125 -40 ~ +125	°C °C
Storage Temperature Range	T <sub>STG</sub>	-65 ~ +150	°C

#### LM7805/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit,  $T_{MIN} < T_J < T_{MAX}$ ,  $I_O = 500$  mA,  $V_I = 10$ V,  $C_I = 0.33 \mu$ F,  $C_O = 0.1 \mu$ F, unless otherwise specified)

Characteristic	Symbol	Test Conditions	L	M780	5I	L	.M780	Unit		
Characteristic	Syllibol	16	si Conditions	Min	Тур	Max	Min	Тур	Max	Ollit
		T <sub>J</sub> =+25 °C		4.8	5.0	5.2	4.8	5.0	5.2	
Output Voltage	Vo	$5.0\text{mA} \le I_{O}$	≤1.0A, P <sub>O</sub> ≤15W							V
		$V_1 = 7V \text{ to } 2$	20V				4.75	5.0	5.25	
		$V_1 = 8V \text{ to } 2$		4.75	5.0	5.25				
Line Regulation	$\Delta V_{\Omega}$	T .0500	$V_0 = 7V \text{ to } 25V$ $V_1 = 8V \text{ to } 12V$		4.0	100		4.0	100	mV
	Δνο	1J=+25°C	$V_I = 8V$ to 12V		1.6	50		1.6	50	IIIV
Load Pagulation	$\Delta V_{\Omega}$	T _ 125°C	I <sub>O</sub> = 5.0mA to 1.5A		9	100		9	100	mV
Load Regulation	Δνο	1J=+25 C	I <sub>O</sub> =250mA to 750mA		4	50		4	50	IIIV
Quiescent Current	Ιq	T <sub>J</sub> =+25 °C			5.0	8		5.0	8	mA
		$I_0 = 5 \text{mA to}$	1.0A		0.03	0.5		0.03	0.5	
Quiescent Current Change	$\Delta I_Q$	$V_I = 7V$ to 2	5V					0.3	1.3	mA
		$V_I = 8V \text{ to } 2$	5V		0.3	1.3				
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_O = 5mA$			-0.8			-0.8		mV/°C
Output Noise Voltage	$V_N$	f = 10Hz to	100Khz, T <sub>A</sub> =+25 °C		42			42		μV/Vo
Ripple	RR	f = 120Hz		62	73		62	73		dB
Rejection	KK	$V_0 = 8 \text{ to } 1$	8V	62	73		02	73		ив
Dropout Voltage	Vo	$I_O = 1A, T_J$	=+25 °C		2			2		V
Output Resistance	Ro	f = 1KHz			15			15		$m\Omega$
Short Circuit Current	I <sub>sc</sub>	$V_1 = 35V, T$	<sub>A</sub> =+25 °C		230			230		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+25 °C			2.2			2.2		Α

<sup>\*</sup> T<sub>MIN</sub> < T<sub>J</sub> < T<sub>MAX</sub> LM78XXI/RI: T<sub>MIN</sub>= - 40 °C, T<sub>MAX</sub> = +125 °C LM78XX/R: T<sub>MIN</sub>= 0 °C, T<sub>MAX</sub>= +125 °C



<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Changes in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

#### LM7806/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit,  $T_{MIN} < T_J < T_{MAX}$ ,  $I_O = 500 mA$ ,  $V_I = 11 V$   $C_I = 0.33 \mu F$ ,  $C_O = 0.1 \mu F$ , unless otherwise specified)

Characteristic	Symbol	т.	st Conditions	L	M7806	l		Unit		
Characteristic	Syllibol	res	st Conditions	Min	Тур	Max	Min	Тур	Max	Unit
		T <sub>J</sub> =+25 °C		5.75	6.0	6.25	5.75	6.0	6.25	
Output Voltage	Vo	5.0mA ≤ I <sub>0</sub> :	≤1.0A, P <sub>D</sub> ≤15W							V
		$V_1 = 8.0V \text{ to}$	21V				5.7	6.0	6.3	
		$V_1 = 9.0V \text{ to}$		5.7	6.0	6.3				
Line Regulation	$\Delta V_{\Omega}$	T <sub>J</sub> =+25 °C	$V_1 = 8V \text{ to } 25V$		5	120		5	120	mV
Zino regulation		1j=120 O	$V_I = 9V$ to $13V$		1.5	60		1.5	60	
Load Regulation	$\Delta V_{\Omega}$	T <sub>.1</sub> =+25 °C	$I_0$ =5mA to 1.5A		9	120		9	120	mV
	2.0	1 <sub>J</sub> =+25 C	I <sub>O</sub> =250mA to750A		3	60		3	60	111.4
Quiescent Current	lα	T <sub>J</sub> =+25 °C			5.0	8		5.0	8	mA
		$I_0 = 5mA$ to	1A			0.5			0.5	
Quiescent Current Change	$\Delta I_Q$	$V_1 = 8V \text{ to } 2$	5V						1.3	mA
		$V_1 = 9V \text{ to } 2$	5V			1.3				
Output Voltage Drift	$\Delta V_O/\Delta T$	$I_0 = 5mA$			-0.8			-0.8		mV/°C
Output Noise Voltage	$V_N$	f = 10Hz to	100Khz, T <sub>A</sub> =+25 °C		45			45		$\mu V/V_O$
Ripple	RR	f = 120Hz		59	75		59	75		dB
Rejection	1	$V_1 = 9V \text{ to } 1$	9V	- 00			00			
Dropout Voltage	$V_D$	$I_0 = 1A, T_J =$	=+25 °C		2			2		V
Output Resistance	$R_D$	f = 1KHz			19			19		mΩ
Short Circuit Current	I <sub>sc</sub>	$V_I = 35V, T_A$	=+25°C		250			250		mA
Peak Current	$I_{PK}$	T <sub>J</sub> =+25 °C			2.2			2.2		Α



<sup>\*</sup>T<sub>MIN</sub> <T<sub>J</sub> <T<sub>MAX</sub>
LM78XXI/RI: T<sub>MIN</sub>= - 40 °C, T<sub>MAX</sub> = +125 °C
LM78XXI/R: T<sub>MIN</sub>= 0 °C, T<sub>MAX</sub>= +125 °C
\*Load and line regulation are specified at constant, junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

#### LM7808/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test Circuit,  $T_{MIN} < T_{J} < T_{MAX}$ ,  $I_{O} = 500$  mA,  $V_{I} = 14$ V,  $C_{I} = 0.33 \mu$ F,  $C_{O} = 0.1 \mu$ F, unless otherwise specified)

Characteristic	Symbol	т.	st Conditions		LM780	)8I		LM780	Unit	
Characteristic	Syllibol	Te	St Conditions	Min	Тур	Max	Min	Тур	Max	Unit
		T <sub>J</sub> =+25 °C		7.7	8.0	8.3	7.7	8.0	8.3	
Output Voltage	Vo	$5.0\text{mA} \le I_{O}$	≤ 1.0A, P <sub>O</sub> ≤ 15W							V
		$V_1 = 10.5V$	to 23V				7.6	8.0	8.4	
		$V_1 = 11.5V$	to 23V	7.6	8.0	8.4				
Line Regulation	$\Delta V_{\Omega}$	T <sub>1</sub> =+ 25°C	V <sub>I</sub> = 10.5V to 25V		5.0	160		5.0	160	mV
Line Regulation	1.0	., . 20 0	$V_I = 11.5V \text{ to } 17V$		2.0	80		2.0	80	IIIV
Load Regulation	$\Delta V_{\Omega}$	T. – ±25°C	$I_0 = 5.0 \text{mA} \text{ to } 1.5 \text{A}$ $I_0 = 250 \text{mA} \text{ to } 750 \text{mA}$		10	160		10	160	mV
Load Regulation	1.0	1J = +23 C	I <sub>O</sub> = 250mA to 750mA		5.0	80		5.0	80	111 V
Quiescent Current	ΙQ	T <sub>J</sub> =+25 °C			5.0	8		5.0	8	mA
		$I_0 = 5 \text{mA to}$	1.0A		0.05	0.5		0.05	0.5	
Quiescent Current Change	$\Delta I_Q$	$V_1 = 10.5A$	to 25V					0.5	1.0	mA
		V <sub>I</sub> = 11.5V	to 25V		0.5	1.0				
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$			-0.8			-0.8		mV/°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to	100Khz, T <sub>A</sub> =+25 °C		52			52		μV/Vo
Ripple	DD	f _ 120Uz	V <sub>I</sub> = 11.5V to 21.5		70			70		ī
Rejection	RR	1 = 120 \(\tau\),	V = 11.5V t0 21.5	56	73		56	73		dB
Dropout Voltage	$V_D$	I <sub>O</sub> = 1A, T <sub>J</sub> :	=+25 °C		2			2		V
Output Resistance	Ro	f = 1KHz			17			17		mΩ
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = 35V, T <sub>A</sub>	√ =+25 °C		230			230		mA
Peak Current	$I_{PK}$	T <sub>J</sub> =+25 °C			2.2			2.2		Α

 $T_{MIN} < T_{J} < T_{MAX}$ 



LM78XX//RI: T<sub>MIN</sub>= - 40 °C, T<sub>MAX</sub> = +125 °C
LM78XX//R: T<sub>MIN</sub>= 0 °C, T<sub>MAX</sub>= +125 °C
\* Load and line regulation are specified at constant, junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

#### LM7809/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit.  $T_{MIN} < T_J < T_{MAX}$ ,  $I_O = 500$  mA,  $V_I = 15$ V,  $C_I = 0.33$  $\mu$ F,  $C_O = 0.1$  $\mu$ F. unless otherwise specified)

Characteristic	Symbol	т	est Conditions	L	M780	91	L	.M780	9	Unit
Characteristic	Syllibol	11	est Conditions	Min	Тур	Max	Min	Тур	Max	Offic
		T <sub>J</sub> =+25 °C		8.65	9	9.35	8.65	9	9.35	
Output Voltage	Vo	$V_{i}$ = 11.5V t	to 24V	8.6	9	9.4	8.6	9	9.4	V
Line Regulation	$\Delta V_{O}$	T .05.00	$V_1 = 11.5V \text{ to } 25V$ $V_1 = 12V \text{ to } 25V$		6	180		6	180	mV
Line Regulation					2	90		2	90	IIIV
Load Regulation	$\Delta V_{\Omega}$	T25°C	$I_0 = 5\text{mA} \text{ to } 1.5\text{A}$		12	180		12	180	mV
Load Regulation	200	1 J=+25 C	$I_0 = 250 \text{mA} \text{ to } 750 \text{mA}$		4	90		4	90	111.0
Quiescent Current	Ιq	T <sub>J</sub> =+25 °C			5.0	8		5.0	8	mA
		$I_0 = 5mA to$	1.0A			0.5			0.5	
Quiescent Current Change	$\Delta I_Q$	$V_1 = 11.5V$	to 26V						1.3	mA
		$V_1 = 12.5V$	to 26V			1.3				
Output Voltage Drift	$\Delta V_O/\Delta T$	$I_0 = 5mA$			-1			-1		mV/°C
Output Noise Voltage	$V_N$	f = 10Hz to	100Khz, T <sub>A</sub> =+25 °C		58			58		μV/V <sub>O</sub>
Ripple Rejection	RR	f = 120Hz $V_1 = 13V$ to	23V	56	71		56	71		dB
Dropout Voltage	$V_D$	$I_0 = 1A, T_J = 1$	=+25 °C		2			2		V
Output Resistance	Ro	f = 1KHz			17			17		mΩ
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = 35V, T	<sub>A</sub> =+25 °C		250			250		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> = +25 °C			2.2			2.2		Α



<sup>\*</sup>  $T_{MIN}$  <  $T_{J}$  <  $T_{MAX}$  LM78XXI/RI:  $T_{MIN}$  = - 40 °C,  $T_{MAX}$  = +125 °C LM78XXI/R:  $T_{MIN}$  = 0 °C,  $T_{MAX}$  = +125 °C \* Load and line regulation are specified at constant, junction temperature. Change in  $V_{O}$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.

#### LM7810/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit,  $T_{MIN} < T_J < T_{MAX}$ ,  $I_O = 500$  mA,  $V_I = 16$  V,  $C_I = 0.33 \mu F$ ,  $C_O = 0.1 \mu F$ , unless otherwise specified)

Characteristic	Cumbal	_			LM78	101		LM78	10	Unit
Characteristic	Symbol	16	est Conditions	Min	Тур	Max	Min	Тур	Max	Unit
		T <sub>J</sub> =+25 °C		9.6	10	10.4	9.6	10	10.4	
Output Voltage	Vo	$5.0\text{mA} \leq I_{0}$	≤1.0A, P <sub>D</sub> ≤15W							V
		$V_1 = 12.5V$	to 25V				9.5	10	10.5	
		$V_1 = 13.5V t$		9.5	10	10.5				
Line Regulation	41/	T±25°C	V <sub>I</sub> = 12.5V to 25V		10	200		10	200	.,
Line regulation	$\Delta V_{O}$	1j=+25 C	$V_1 = 13V \text{ to } 25V$		3	100		3	100	mV
Load Regulation	$\Delta V_{\Omega}$	T±25°C	I <sub>O</sub> = 5mA to 1.5A		12	200		12	200	mV
Load Regulation	Δνο	1J = +23 C	I <sub>O</sub> = 250mA to 750mA		4	400		4	400	1111
Quiescent Current	ΙQ	T <sub>J</sub> =+25 °C			5.1	8		5.1	8	mA
		$I_0 = 5mA to$	1.0A			0.5			0.5	
Quiescent Current Change	$\Delta I_Q$	$V_1 = 12.5V$	to 29V						1.0	mA
		$V_1 = 13.5V$	to 29V			1.0				
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$			-1			-1		mV/°C
Output Noise Voltage	$V_N$	f = 10Hz to	100Khz, T <sub>A</sub> =+25 °C		58			58		μV/Vo
Ripple	RR	f = 120Hz		56	71		56	71		dB
Rejection	KK	$V_1 = 13V \text{ to}$	23V	50	71		56	71		иь
Dropout Voltage	$V_D$	$I_0 = 1A, T_{J^2}$	=+25 °C		2			2		V
Output Resistance	Ro	f = 1KHz	•		17			17		mΩ
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = 35V, T	<sub>A</sub> =+25 °C		250			250		mA
Peak Current	$I_{PK}$	T <sub>J</sub> =+25 °C			2.2	·		2.2		Α

 $T_{MIN} < T_{J} < T_{MAX}$ 



LM78XX//RI: T<sub>MIN</sub>= - 40 °C, T<sub>MAX</sub> = +125 °C
LM78XX//R: T<sub>MIN</sub>= 0 °C, T<sub>MAX</sub>= +125 °C
\* Load and line regulation are specified at constant, junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

#### LM7811/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit,  $T_{MIN} < T_J < T_{MAX}$ ,  $I_O = 500 mA$ ,  $V_I = 18 V$ ,  $C_I = 0.33 \mu F$ ,  $C_O = 0.1 \mu F$ , unless otherwise specified)

Characteristic	Cumbal	Total Constitution		LM781	1 <b>1</b>		LM78	11	
Characteristic	Symbol	Test Conditions	Min	Тур	Max	Min	Тур	Max	Unit
		T <sub>J</sub> =+25 °C	10.6	11	11.4	10.6	11	11.4	
Output Voltage	Vo	$5.0 \text{mA} \le I_0 \le 1.0 \text{A}, P_0 \le 15 \text{W}$							V
		V <sub>I</sub> = 13.5V to 26V				10.5	11	11.5	
		V <sub>I</sub> = 14.5V to 26V	10.5	11	11.5				
Line Regulation	437	$T_J = +25^{\circ}C$ $\frac{V_I = 13.5 \text{V to } 25 \text{V}}{V_I = 14 \text{V to } 21 \text{V}}$		10	220		10	220	\/
	$\Delta V_{O}$	$V_1 = 14V \text{ to } 21V$		3.0	110		3	110	mV
Load Regulation	$\Delta V_{O}$	$T_{.1} = +25^{\circ}C$ $I_0 = 5.0 \text{mA to } 1.5 \text{A}$		12	220		12	220	mV
Load (togulation	70	$I_0 = 250 \text{mA} \text{ to } 750 \text{mA}$		4	110		4	110	
Quiescent Current	ΙQ	T <sub>J</sub> =+25 °C		5.1	8		5.1	8	mA
		$I_O = 5$ mA to 1.0A			0.5			0.5	
Quiescent Current Change	$\Delta I_Q$	$V_1 = 13.5V$ to 29V						1.0	mA
		V <sub>I</sub> = 14.5V to 29V			1.0				
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_O = 5mA$		-1			-1		mV/°C
Output Noise Voltage	$V_N$	f = 10Hz to 100Khz, T <sub>A</sub> =+25 °C		70			70		$\mu V/V_O$
Ripple	RR	f = 120Hz	55	71		55	71		dB
Rejection	KK	V <sub>I</sub> = 14V to 24V	ວວ	71		55	71		ив
Dropout Voltage	$V_D$	I <sub>O</sub> = 1A, T <sub>J</sub> =+25 °C		2			2		V
Output Resistance	Ro	f = 1KHz		18			18		mΩ
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = 35V, T <sub>A</sub> =+25 °C		250	•		250		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+25 °C		2.2	•		2.2		Α



<sup>\*</sup>T<sub>MIN</sub> <T<sub>J</sub> <T<sub>MAX</sub>

LM78XXI/RI: T<sub>MIN</sub>= - 40 °C, T<sub>MAX</sub> = +125 °C

LM78XX/R: T<sub>MIN</sub>= 0 °C, T<sub>MAX</sub>= +125 °C

\*Load and line regulation are specified at constant, junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

#### LM7812/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit,  $T_{MIN} < T_J < T_{MAX}$ ,  $I_O$ =500mA,  $V_I$ =19V,  $C_I$ = 0.33 $\mu$ F,  $C_O$ = 0.1. $\mu$ F, unless otherwise specified)

Characteristic	Symbol	T	est Conditions	I	_M78	121		LM78	12	Unit
Gridiantorionio	Cymbol	•		Min	Тур	Max	Min	Тур	Max	Omi
		T <sub>J</sub> =+25 °C		11.5	12	12.5	11.5	12	12.5	
Output Voltage	Vo	$5.0\text{mA} \leq I_0$	≤1.0A, P <sub>D</sub> ≤15W							V
		$V_1 = 14.5V$	to 27V				11.4	12	12.6	
		$V_{I} = 15.5V1$	to 27V	11.4	12	12.6				
Line Regulation		T+25°C	$V_1 = 14.5 \text{V to } 30 \text{V}$		10	240		10	240	.,
Line Regulation	$\Delta V_{O}$	1j=+25 C	$V_1 = 16V \text{ to } 22V$		3.0	120		3.0	120	mV
Load Regulation	$\Delta V_{\Omega}$	T+25°C	I <sub>O</sub> = 5mA to 1.5A		11	240		11	240	mV
Load Regulation	1.0	11-120 0	I <sub>O</sub> = 250mA to 750mA		5.0	120		5.0	120	1117
Quiescent Current	ΙQ	T <sub>J</sub> =+25 °C	;		5.1	8		5.1	8	mA
		$I_0 = 5mA to$	1.0A		0.1	0.5		0.1	0.5	
Quiescent Current Change	$\Delta I_Q$	$V_1 = 14.5V$	to 30V					0.5	1.0	mA
		$V_1 = 15V tc$	30V			1.0				
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$		0.5	-1			-1		mV/°C
Output Noise Voltage	$V_N$	f = 10Hz to	100Khz, T <sub>A</sub> =+25 °C		76			76		mV/V <sub>O</sub>
Ripple	RR	f = 120Hz		55	71		55	71		dB
Rejection	KK	$V_1 = 15V \text{ to}$	25V	55	71		55	71		иь
Dropout Voltage	$V_D$	$I_0 = 1A, T_J$	=+25 °C		2			2		V
Output Resistance	Ro	f = 1KHz			18			18		mΩ
Short Circuit Current	I <sub>SC</sub>	$V_1 = 35V, T$	<sub>A</sub> =+25 °C		230			230		mA
Peak Current	$I_{PK}$	T <sub>J</sub> = +25 °C			2.2			2.2		Α



 $<sup>\</sup>begin{split} &T_{MIN}\!<\!T_{J}\!<\!T_{MAX}\\ &LM78XXI/RI:T_{MIN}\!=\!-40\,^{\circ}C,\,T_{MAX}\!=\!+125\,^{\circ}C\\ &LM78XXI/R:T_{MIN}\!=\!0\,^{\circ}C,\,T_{MAX}\!=\!+125\,^{\circ}C\\ &^{*}Load \ and \ line\ regulation\ are\ specified\ at\ constant,\ junction\ temperature.\ Change\ in\ V_{O}\ due\ to\ heating\ effects\ must\ be\ taken\ into\ account\ separately.\ Pulse\ testing\ with\ low\ duty\ is\ used. \end{split}$ 

#### LM7815/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit,  $T_{MIN} < T_J < T_{MAX}$ ,  $I_O$  =500mA,  $V_I$  =23V,  $C_I$  =0.33 $\mu$ F,  $C_O$  =0.1 $\mu$ F, unless otherwise specified)

Characteristic	Cumbal	I Test Conditions		LM781	151	L	LM7815			
Characteristic	Symbol	16	est Conditions	Min	Тур	Max	Min	Тур	Max	Unit
		T <sub>J</sub> =+25 °C		14.4	15	15.6	14.4	15	15.6	
Output Voltage	Vo	$5.0\text{mA} \le I_{O}$	≤1.0A, P <sub>D</sub> ≤15W							V
		$V_1 = 17.5V$	to 30V	14.2	15	15.75	14.25	15	15.75	
		$V_{I}$ = 18.5V t		5						
Line Regulation		T <sub>1</sub> =+25°C	V <sub>I</sub> = 17.5V to 30V		11	300		11	300	\/
Line Regulation	$\Delta V_{O}$	13 = 120 0	$V_1 = 20V \text{ to } 26V$		3	150		3	150	mV
Load Regulation	$\Delta V_{O}$		$I_0 = 5mA \text{ to } 1.5A$ $I_0 = 250mA \text{ to } 750mA$		12	300		12	300	mV
Load Regulation	40	T <sub>J</sub> =+25°C	$I_0 = 250 \text{mA}$ to 750 mA		4	150		4	150	
Quiescent Current	ΙQ	T <sub>J</sub> =+25 °C			5.2	8		5.2	8	mA
		$I_0 = 5mA to$	1.0A			0.5			0.5	
Quiescent Current Change	$\Delta I_Q$	$V_1 = 17.5V$	to 30V						1.0	mA
		$V_1 = 18.5V$	to 30V			1.0				
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$			-1			-1		mV/°C
Output Noise Voltage	$V_N$	f = 10Hz to	100Khz, T <sub>A</sub> =+25 °C		90			90		$\mu V/V_O$
Ripple	RR	f = 120Hz		54	70		54	70		dB
Rejection	KK	$V_1 = 18.5V$	to 28.5V	54	70		54	70		uБ
Dropout Voltage	$V_D$	$I_0 = 1A, T_J$	=+25 °C		2			2		V
Output Resistance	Ro	f = 1KHz			19			19		mΩ
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = 35V, T	<sub>A</sub> =+25 °C		250			250		mA
Peak Current	$I_{PK}$	T <sub>J</sub> =+25 °C			2.2			2.2		Α



 $<sup>^{\</sup>star}T_{\text{MIN}} < T_{\text{J}} < T_{\text{MAX}} \\ \text{LM78XXI/RI: } T_{\text{MIN}} = -40\,^{\circ}\text{C}, T_{\text{MAX}} = +125\,^{\circ}\text{C} \\ \text{LM78XXI/R: } T_{\text{MIN}} = 0\,^{\circ}\text{C}, T_{\text{MAX}} = +125\,^{\circ}\text{C} \\ ^{\star}\text{Load} \text{ and line regulation are specified at constant, junction temperature. Change in $V_{\text{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.}$ 

#### LM7818/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit,  $T_{MIN} < T_J < T_{MAX}$ ,  $I_O$  =500mA,  $V_I$  =27V,  $C_I$  =0.33 $\mu$ F,  $C_O$  =0.1 $\mu$ F, unless otherwise specified)

Characteristic	Symbol	T	est Conditions	I	LM781	<b>8</b> I		LM78	18	Unit
Characteristic	Syllibol	10	est Conditions	Min	Тур	Max	Min	Тур	Max	Onit
		T <sub>J</sub> =+25 °C		17.3	18	18.7	17.3	18	18.7	
Output Voltage	Vo	$5.0\text{mA} \leq I_{O}$	≤1.0A, P <sub>D</sub> ≤15W							V
		$V_I = 21V \text{ to}$	33V				17.1	18	18.9	
		$V_I = 22V$ to		17.1	18	18.9				
Line Regulation		T+25°C	$V_1 = 21V \text{ to } 33V$ $V_1 = 24V \text{ to } 30V$		15	360		15	360	.,
Line Regulation	$\Delta V_{O}$	11 = 120 0	$V_1 = 24V \text{ to } 30V$		5	180		5	180	mV
Load Regulation	$\Delta V_{\Omega}$	T+25°C	$I_0 = 5 \text{mA to } 1.5 \text{A}$ $I_0 = 250 \text{mA to } 750 \text{mA}$		15	360		15	360	mV
Load (togulation	Δνο	1 J = 120 O	$I_0 = 250 \text{mA} \text{ to } 750 \text{mA}$		5.0	180		5.0	180	
Quiescent Current	ΙQ	T <sub>J</sub> =+25 °C			5.2	8		5.2	8	mA
		$I_0 = 5mA to$	1.0A			0.5			0.5	
Quiescent Current Change	$\Delta I_Q$	$V_1 = 21V \text{ to}$	33V						1	mA
		$V_I = 22V to$	33V			1.0				
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$			-1			-1		mV/°C
Output Noise Voltage	$V_N$	f = 10Hz to	100Khz, T <sub>A</sub> =+25 °C		110			110		μV/V <sub>O</sub>
Ripple	RR	f = 120Hz		53	69		53	69		dB
Rejection	KK	$V_I = 22V to$	32V	53	69		53	69		uБ
Dropout Voltage	$V_D$	$I_0 = 1A, T_{J^2}$	=+25 °C		2			2		V
Output Resistance	Ro	f = 1KHz			22			22		mΩ
Short Circuit Current	I <sub>SC</sub>	V <sub>I</sub> = 35V, T	<sub>A</sub> =+25 °C		250			250		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+25 °C			2.2			2.2		Α

 $T_{MIN} < T_{J} < T_{MAX}$ 



IMIN < I J < I MAX LM78XXI/RI: T<sub>MIN</sub>= - 40 °C, T<sub>MAX</sub> = +125 °C LM78XX/R: T<sub>MIN</sub>= 0 °C, T<sub>MAX</sub>= +125 °C \* Load and line regulation are specified at constant, junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

#### LM7824/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to test circuit,  $T_{MIN} < T_J < T_{MAX}$ ,  $I_O = 500 \text{mA}$ ,  $V_I = 33 \text{V}$ ,  $C_I = 0.33 \mu\text{F}$ ,  $C_O = 0.1 \mu\text{F}$ , unless otherwise specified)

Characteristic	Symbol	Test Conditions	I	_M782	241		Unit		
Characteristic	Syllibol	rest Conditions	Min	Тур	Max	Min	Тур	Max	Unit
		T <sub>J</sub> =+25 °C	23	24	25	23	24	25	
Output Voltage	Vo	$5.0 \text{mA} \le I_0 \le 1.0 \text{A}, P_0 \le 15 \text{W}$							V
		V <sub>I</sub> = 27V to 38V				22.8	24	25.25	
		V <sub>I</sub> = 28V to 38V	22.8	24	25.2				
Line Regulation		$T_J = +25^{\circ}C$ $\frac{V_I = 27V \text{ to } 38V}{V_I = 30V \text{ to } 36V}$		17	480		17	480	
Line Regulation	$\Delta V_{O}$	$V_1 = 425^{\circ} \text{C}$ $V_1 = 30 \text{V} \text{ to } 36 \text{V}$		6	240		6	240	mV
Load Regulation	$\Delta V_{O}$	$T_J = +25^{\circ}C$ $I_O = 5mA \text{ to } 1.5A$		15	480		15	480	mV
Load Regulation	Δ.0	$I_0 = 250 \text{mA}$ to 750 mA		5.0	240		5.0	240	IIIV
Quiescent Current	ΙQ	T <sub>J</sub> =+25 °C		5.2	8		5.2	8	mA
		$I_O = 5$ mA to 1.0A		0.1	0.5		0.1	0.5	
Quiescent Current Change	$\Delta I_Q$	V <sub>I</sub> = 27V to 38V					0.5	1	mA
		V <sub>I</sub> = 28V to 38V		0.5	1				
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_O = 5mA$		-1.5			-1.5		mV/°C
Output Noise Voltage	$V_N$	f = 10Hz to 100KHz, T <sub>A</sub> =+25 °C		160			60		$\mu V/V_O$
Ripple	RR	f = 120Hz	50	67		50	67		40
Rejection	KK	$V_I = 28V$ to $38V$	50	67		50	67		dB
Dropout Voltage	$V_D$	I <sub>O</sub> = 1A, T <sub>J</sub> =+25 °C		2			2		V
Output Resistance	Ro	f = 1KHz		28			28		mΩ
Short Circuit Current	I <sub>SC</sub>	$V_1 = 35V, T_A = +25 ^{\circ}C$		230			230		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+25 °C		2.2			2.2		Α



 $<sup>^{\</sup>star}T_{\text{MIN}} < T_{\text{J}} < T_{\text{MAX}} \\ \text{LM78XXI/RI: } T_{\text{MIN}} = -40\,^{\circ}\text{C}, T_{\text{MAX}} = +125\,^{\circ}\text{C} \\ \text{LM78XXI/R: } T_{\text{MIN}} = 0\,^{\circ}\text{C}, T_{\text{MAX}} = +125\,^{\circ}\text{C} \\ ^{\star}\text{Load} \text{ and line regulation are specified at constant, junction temperature. Change in $V_{\text{O}}$ due to heating effects must be taken into account separately. Pulse testing with low duty is used.}$ 

#### LM7805A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits.  $T_J = 0$  to +I25 °C,  $I_O = 1A$ ,  $V_I = 10V$ ,  $C_I = 0.33 \mu F$ ,  $C_O = 0.1 \mu F$ , unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> =+25 °C	4.9	5	5.1	
Output Voltage	Vo	$I_0 = 5mA \text{ to } 1A, P_D \le 5W$ $V_1 = 7.5 \text{ to } 20V$	4.8	5	5.2	V
		$V_1 = 7.5 \text{ to } 25V$		5	50	
		I <sub>O</sub> = 500mA				
Line Regulation	$\Delta V_{O}$	V <sub>I</sub> = 8V to 12V		3	50	V
		T <sub>J</sub> =+25 °C	/	5	50	
		V <sub>I</sub> = 8V to 12V		1.5	25	
		T <sub>J</sub> =+25 °C		9	100	
Lood Dogulation	$\Delta V_{O}$	$I_0 = 5$ mA to 1.5A				V
Load Regulation	2,0	$I_0 = 5 \text{mA to } 1 \text{A}$		9	100	V
		I <sub>O</sub> = 250 to 750mA		4	50	
Quiescent Current	ΙQ	T <sub>J</sub> =+25 °C		5.0	6	mA
		$I_0 = 5 \text{mA to } 1 \text{A}$			0.5	
Quiescent Current Change	$\Delta I_Q$	$V_1 = 8 \text{ V to } 25\text{V}, I_0 = 500\text{mA}$			8.0	mA
		$V_I = 7.5 \text{V to } 20 \text{V}, T_J = +25 ^{\circ}\text{C}$			0.8	
Output Voltage Drift	ΔV/ΔΤ	$I_0 = 5mA$		-0.8		mV/°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to 100KHz T <sub>A</sub> =+25 °C		10		μV/V <sub>O</sub>
Ripple Rejection	RR	$f = 120Hz, I_0 = 500mA$ V <sub>I</sub> = 8V to 18V		68		dB
Dropout Voltage	V <sub>D</sub>	I <sub>O</sub> = 1A, T <sub>J</sub> =+25 °C		2		V
Output Resistance	Ro	f = 1KHz		17		mΩ
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = 35V, T <sub>A</sub> =+25 °C		250		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> = +25 °C		2.2		Α

 $<sup>^*</sup>$ Load and line regulation are specified at constant, junction temperature. Change in  $V_0$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.



### LM7806A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits.  $T_J = 0$  to+150 °C,  $I_O = 1$ A,  $V_I = 11$ V,  $C_I = 0.33 \mu F$ ,  $C_O = 0.1 \mu F$ , unless otherwise specified)

Characteristic	Symbol	Test Conditio	ns Min	Тур	Max	Unit
		T <sub>J</sub> =+25 °C	5.58	6	6.12	
Output Voltage	Vo	$I_O = 5mA \text{ to } 1A, P_D \le 15$ $V_I = 8.6 \text{ to } 21V$	5W 5.76	6	6.24	V
		V <sub>I</sub> = 8.6 to 25V I <sub>O</sub> = 500mA		5	60	
Line Regulation	$\Delta V_{O}$	V <sub>I</sub> = 9V to 13V		3	60	mV
		T <sub>J</sub> =+25 °C	o 21V	5	60	
		$V_i = 9V \text{ to}$	13V	1.5	30	
		$T_J = +25 ^{\circ}\text{C}$ $I_O = 5\text{mA to } 1.5\text{A}$		9	100	.,
Load Regulation	$\Delta V_{O}$	$I_0 = 5 \text{mA to } 1 \text{A}$		4	100	mV
		I <sub>O</sub> = 250 to 750mA		5.0	50	
Quiescent Current	ΙQ	T <sub>J</sub> =+25 °C		4.3	6	mA
		$I_O = 5mA$ to 1A			0.5	
Quiescent Current Change	$\Delta I_{Q}$	$V_1 = 9V \text{ to } 25V, I_0 = 500$	OmA		0.8	mA
		$V_1 = 8.5 \text{V to } 21 \text{V}, T_J = +2$	25 °C		0.8	
Output Voltage Drift	ΔV/ΔΤ	$I_O = 5mA$		-0.8		mV/°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to $100KHzT_A = +25 °C$		10		μ V/V <sub>O</sub>
Ripple Rejection	RR	$f = 120Hz, I_0 = 500mA$ $V_1 = 9V \text{ to } 19V$		65		dB
Dropout Voltage	V <sub>D</sub>	I <sub>O</sub> = 1A, T <sub>J</sub> =+25 °C		2		V
Output Resistance	Ro	f = 1KHz		17		mΩ
Short Circuit Current	I <sub>SC</sub>	V <sub>I</sub> = 35V, T <sub>A</sub> =+25 °C		250		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+25 °C		2.2		Α

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant, junction temperature. Change in  $V_{\text{O}}$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.



### LM7808A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits.  $T_J = 0$  to+150 °C,  $I_O = 1$ A,  $V_I = 14$ V,  $C_I = 0.33 \mu F$ ,  $C_O = 0.1 \mu F$ , unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> =+25 °C	7.84	8	8.16	
Output Voltage	Vo	$I_{O} = 5mA \text{ to } 1A, P_{D} \le 15W$ V <sub>I</sub> = 8.6 to 21V	7.7	8	8.3	٧
		V <sub>I</sub> = 10.6 to 25V I <sub>O</sub> = 500mA		6	80	
Line Regulation	$\Delta V_{O}$	V <sub>I</sub> = 11to 17V		3	80	mV
		T <sub>J</sub> =+25 °C V <sub>I</sub> = 10.4V to 23V		6	80	
		V <sub>I</sub> = 11V to 17V		2	40	
		$T_J = +25 ^{\circ}\text{C}$ $I_O = 5\text{mA to } 1.5\text{A}$		12	100	
Load Regulation	$\Delta V_{O}$	I <sub>O</sub> = 5mA to 1A		12	100	mV
		I <sub>O</sub> = 250 to 750mA		5	50	
Quiescent Current	lα	T <sub>J</sub> =+25 °C		5.0	6	mA
		$I_0 = 5mA$ to 1A			0.5	
Quiescent Current Change	$\Delta I_Q$	$V_1 = 11V$ to 25V, $I_0 = 500$ mA			0.8	mA
		$V_I$ = 10.6V to 23V, $T_J$ =+25 °C			0.8	
Output Voltage Drift	ΔV/ΔΤ	I <sub>O</sub> = 5mA		-0.8		mV /°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to $100$ KHz $T_A = +25$ °C		10		μV/V <sub>O</sub>
Ripple Rejection	RR	$f = 120Hz, I_0 = 500mA$ V <sub>I</sub> = 11.5V to 21.5V		62		dB
Dropout Voltage	V <sub>D</sub>	I <sub>O</sub> = 1A, T <sub>J</sub> =+25 °C		2		V
Output Resistance	Ro	f = 1KHz		18		mΩ
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = 35V, T <sub>A</sub> =+25°C		250		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+25 °C		2.2		Α

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant, junction temperature. Change in  $V_{O}$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.



### LM7809A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits.  $T_J = 0$  to +125 °C,  $I_O = 1$ A,  $V_I = 15$ V,  $C_I = 0.33 \mu F$ ,  $C_O = 0.1 \mu F$ , unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Тур	Max	Unit
		T <sub>J</sub> =+25 °C		8.82	9.0	9.18	
Output Voltage	Vo	ŭ	$I_0 = 5\text{mA to 1A}, P_D \le 15\text{W}$ $V_1 = 11.2 \text{ to } 24\text{V}$		9.0	9.35	V
		$V_1 = 11.7 \text{ to } 2000 \text{ s}$ $I_0 = 500 \text{ mA}$	25V		6	90	
Line Regulation	$\Delta V_{O}$	$V_{I}$ = 12.5 to 1	9V		4	45	mV
		T <sub>J</sub> =+25 °C	$V_{I}$ = 11.5V to 24V		6	90	
		1j=+25 C	V <sub>I</sub> = 12.5V to 19V		2	45	
Land Danielation		$T_J = +25 ^{\circ}\text{C}$ $I_O = 5\text{mA to}$	1.0A		12	100	.,
Load Regulation	$\Delta V_{O}$	$I_0 = 5 \text{mA to}$	$I_O = 5$ mA to 1.0A		12	100	mV
		$I_0 = 250 \text{ to } 7$	50mA		5	50	
Quiescent Current	ΙQ	T <sub>J</sub> =+25 °C			5.0	6.0	mA
		$V_1 = 11.7V \text{ to}$	25V, T <sub>J</sub> =+25 °C			8.0	
Quiescent Current Change	$\Delta I_Q$	$V_1 = 12V \text{ to } 25V, I_0 = 500\text{mA}$				0.8	mA
		$I_0 = 5mA$ to	1.0A			0.5	
Output Voltage Drift	ΔV/ΔΤ	$I_O = 5mA$			-1.0		mV/°C
Output Noise Voltage	V <sub>N</sub>	$f = 10Hz$ to $T_A = +25$ °C	100KHz		10		μV/V <sub>O</sub>
Ripple Rejection	RR	f = 120Hz, I <sub>O</sub> = 500mA V <sub>I</sub> = 12V to 22V			62		dB
Dropout Voltage	$V_D$	I <sub>O</sub> = 1A, T <sub>J</sub> =+25 °C			2.0		V
Output Resistance	Ro	f = 1KHz			17		mΩ
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = 35V, T <sub>A</sub>	=+25 °C		250		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+25 °C			2.2		Α

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant, junction temperature. Change in  $V_{O}$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.



### LM7810A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits.  $T_J = 0$  to+125 °C,  $I_O = 1A$ ,  $V_I = 16V$ ,  $C_I = 0.33 \mu F$ ,  $C_O = 0.1 \mu F$ , unless otherwise specified)

Characteristic	Symbol	Test	Conditions	Min	Тур	Max	Unit	
		T <sub>J</sub> =+25 °C		9.8	10	10.2		
Output Voltage	Vo	$I_{O} = 5mA \text{ to } 1A, P_{D} \le 15W$ $V_{I} = 12.8 \text{ to } 25V$		9.6	10	10.4	V	
		$V_{I}$ = 12.8 to 2 $I_{O}$ = 500mA	6V		8	100		
Line Regulation	$\Delta V_{O}$	V <sub>I</sub> = 13to 20V	!		4	50	mV	
		T <sub>J</sub> =+25 °C	V <sub>I</sub> = 12.5V to 25V		8	100		
		13-120 0	V <sub>I</sub> = 13V to 20V		3	50		
Load Regulation	A)/	$T_J = +25 ^{\circ}\text{C}$ $I_O = 5\text{mA to}$	1.5A		12	100		
Load Regulation	Δνο	ΔVo	$I_0 = 5 \text{mA to}$	1.0A		12	100	mV
		I <sub>O</sub> = 250 to 750mA			5	50		
Quiescent Current	lα	T <sub>J</sub> =+25 °C			5.0	6.0	mA	
		$V_1 = 13V \text{ to } 2$	26V, T <sub>J</sub> =+25 °C			0.5		
Quiescent Current Change	$\Delta I_{Q}$	$V_1 = 12.8V \text{ to } 25V, I_0 = 500\text{mA}$				0.8	mA	
		$I_0 = 5 \text{mA to}$	1.0A			0.5		
Output Voltage Drift	ΔV/ΔΤ	I <sub>O</sub> = 5mA			-1.0		mV °C	
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to 1 T <sub>A</sub> =+25 °C	00KHz		10		μV/V <sub>O</sub>	
Ripple Rejection	RR	f = 120Hz, I <sub>O</sub> = 500mA V <sub>I</sub> = 14V to 24V			62		dB	
Dropout Voltage	$V_D$	I <sub>O</sub> = 1A, T <sub>J</sub> =+25 °C			2.0		V	
Output Resistance	Ro	f = 1KHz			17		mΩ	
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = 35V, T <sub>A</sub>	=+25 °C		250		mA	
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+25 °C			2.2		Α	

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant, junction temperature. Change in  $V_{\text{O}}$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.



### LM7811A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits.  $T_J = 0$  to +125 °C,  $I_O = 1$ A,  $V_I = 18$ V,  $C_I = 0.33 \mu F$ ,  $C_O = 0.1 \mu F$ , unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Тур	Max	Unit
		T <sub>J</sub> =+25 °C		10.8	11.0	11.2	
Output Voltage	Vo		$I_{O} = 5$ mA to 1A, $P_{D} \le 15$ W $V_{I} = 13.8$ to 26V		11.0	11.4	V
		$V_{I}$ = 12.8 to 2 $I_{O}$ = 500mA	26V		10	110	
Line Regulation	$\Delta V_{O}$	V <sub>I</sub> = 15 to 21	V		4	55	mV
		T <sub>1</sub> =+25°C	$V_i$ = 13.5V to 26V		10	110	
		13 120 0	V <sub>I</sub> = 15V to 21V		3	55	
Load Degulation	.,,	$T_J = +25 ^{\circ}\text{C}$ $I_O = 5\text{mA to}$	1.5A		12 100		
Load Regulation	$\Delta V_{O}$	I <sub>O</sub> = 5mA to 1.0A			12	100	mV
		I <sub>O</sub> = 250 to 750mA			5	50	
Quiescent Current	lα	T <sub>J</sub> =+25 °C			5.1	6.0	mA
		$V_1 = 13.8V \text{ to}$	26V, T <sub>J</sub> =+25 °C			0.8	
Quiescent Current Change	$\Delta I_{O}$	$V_1 = 14V \text{ to } 2$	27V, I <sub>O</sub> = 500mA			0.8	mA
		$I_0 = 5 \text{mA to}$	1.0A			0.5	
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$			-1.0		mV /°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to 1 T <sub>A</sub> =+25 °C	00KHz		10		μV/V <sub>O</sub>
Ripple Rejection	RR	f = 120Hz, I <sub>O</sub> = 500mA V <sub>I</sub> = 14V to 24V			61		dB
Dropout Voltage	V <sub>D</sub>	I <sub>O</sub> = 1A, T <sub>J</sub> =+25 °C			2.0		V
Output Resistance	Ro	f = 1KHz			18		mΩ
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = 35V, T <sub>A</sub> :	=+25 °C		250		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+25 °C			2.2		Α

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant, junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.



### LM7812A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits.  $T_J = 0$  to +125 °C,  $I_O = 1A$ ,  $V_I = 19V$ ,  $C_I = 0.33 \mu F$ ,  $C_O = 0.1 \mu F$ , unless otherwise specified)

Characteristic	Symbol	Tes	t Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> =+25 °C		11.75	12	12.25	
Output Voltage	Vo	$I_0 = 5 \text{mA to } 1$ $V_1 = 14.8 \text{ to } 2$	, ,	11.5	12	12.5	٧
		$V_{I}$ = 14.8 to 30 $I_{O}$ = 500mA	0V		10	120	
Line Regulation	$\Delta V_{O}$	V <sub>I</sub> = 16 to 22\	/		4	120	mV
		T <sub>J</sub> =+25°C	$V_{I}$ = 14.5V to 27V		10	120	
		1j =+25 C	$V_{I}$ = 16V to 22V		3	60	
Load Regulation	41/	$T_J = +25^{\circ}C$ $I_O = 5mA \text{ to } 1$	.5A		12	100	
Load Regulation	$\Delta V_{O}$	$I_0 = 5$ mA to 1	.0A		12	100	mV
		$I_0 = 250 \text{ to } 75$	50mA		5	50	
Quiescent Current	lα	T <sub>J</sub> =+25 °C			5.1	6.0	mA
		$V_1 = 15V \text{ to } 3$	0V, T <sub>J</sub> =+25 °C			0.5	
Quiescent Current Change	$\Delta I_{Q}$	$V_1 = 14V \text{ to } 2$	7V, I <sub>O</sub> = 500mA			0.8	mA
		$I_0 = 5$ mA to 1	.0A			0.8	
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$			-1.0		mV/°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz  to  1 $T_A = +25 ^{\circ}\text{C}$	00KHz		10		μV/V <sub>O</sub>
Ripple Rejection	RR	f = 120Hz, I <sub>O</sub> = 500mA V <sub>I</sub> = 14V to 24V			60		dB
Dropout Voltage	$V_D$	I <sub>O</sub> = 1A, T <sub>J</sub> =+25 °C			2.0		V
Output Resistance	Ro	f = 1KHz			18		mΩ
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = 35V, T <sub>A</sub> =	=+25 °C		250		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+25 °C	·		2.2		Α

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant, junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.



### LM7815A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits.  $T_J = 0$  to +150 °C,  $I_O = 1A$ ,  $V_I = 23V$ ,  $C_I = 0.33 \mu F$ ,  $C_O = 0.1 \mu F$ , unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> =+25 °C	14.7	15	15.3	
Output Voltage	Vo	$I_{O} = 5mA \text{ to } 1A, P_{D} \le 15W$ $V_{I} = 17.7 \text{ to } 30V$	14.4	15	15.6	V
		V <sub>I</sub> = 17.9 to 30V I <sub>O</sub> = 500mA		10	150	
Line Regulation	$\Delta V_{O}$	V <sub>I</sub> = 20 to 26V		5	150	mV
		T <sub>J</sub> =+25 °C V <sub>I</sub> = 17.5V to 30V		11	150	
		V <sub>I</sub> = 20V to 26V		3	75	
Load Danidation		$T_J$ =+25 °C $I_O$ = 5mA to 1.5A		12	100	
Load Regulation	$\Delta V_{O}$	I <sub>O</sub> = 5mA to 1.0A		12	100	mV
		I <sub>O</sub> = 250 to 750mA		5	50	
Quiescent Current	lα	T <sub>J</sub> =+25 °C		5.2	6.0	mA
		$V_I = 17.5 \text{V to } 30 \text{V}, T_J = +25 ^{\circ}\text{C}$			0.5	
Quiescent Current Change	$\Delta I_Q$	$V_1 = 17.5V \text{ to } 30V, I_0 = 500\text{mA}$			0.8	mA
		$I_O = 5mA$ to 1.0A			0.8	
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$		-1.0		mV/°C
Output Noise Voltage	$V_N$	f = 10Hz to $100KHzT_A = +25 °C$		10		μV/V <sub>O</sub>
Ripple Rejection	RR	$f = 120Hz, I_0 = 500mA$ $V_1 = 18.5V \text{ to } 28.5V$		58		dB
Dropout Voltage	V <sub>D</sub>	I <sub>O</sub> = 1A, T <sub>J</sub> =+25 °C		2.0		V
Output Resistance	Ro	f = 1KHz		19		mΩ
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = 35V, T <sub>A</sub> =+25 °C		250		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+25 °C		2.2	_	Α

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant, junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.



### LM7818A/RA ELECTRICAL CHARACTERISTICS

(Refer to the test circuits.  $T_J = 0$  to +150 °C,  $I_O = 1A$ ,  $V_I = 27V$ ,  $C_I = 0.33 \mu F$ ,  $C_O = 0.1 \mu F$ , unless otherwise specified)

Characteristic	Symbol	Test Conditions		Min	Тур	Max	Unit
		T <sub>J</sub> =+25 °C		17.64	18	18.36	
Output Voltage	Vo	-	$I_{O} = 5 \text{mA to 1A}, P_{D} \le 15 \text{W}$ $V_{I} = 21 \text{ to } 33 \text{V}$		18	18.7	V
		$V_1 = 21 \text{ to } 33^{\circ}$ $I_0 = 500\text{mA}$	V		15	180	
Line Regulation	$\Delta V_{O}$	V <sub>I</sub> = 21 to 33	V		5	180	mV
		T .25°C	$V_{I}$ = 20.6V to 33V		15	180	
		T <sub>J</sub> =+25 °C	V <sub>I</sub> = 24V to 30V		5	90	
Lood Domidation		$T_J = +25 ^{\circ}\text{C}$ $I_O = 5\text{mA to}$	1.5A	15 100		,	
Load Regulation	$\Delta V_{O}$	$I_0 = 5 \text{mA to}$	1.0A		15	100	mV
		$I_0 = 250 \text{ to } 7$	50mA		7	50	
Quiescent Current	lα	T <sub>J</sub> =+25 °C			5.2	6.0	mA
		$V_1 = 21V \text{ to } 3$	33V, T <sub>J</sub> =+25 °C			0.5	
Quiescent Current Change	$\Delta I_Q$	$V_{I} = 21V \text{ to } 3$	$33V, I_O = 500mA$			0.8	mA
		$I_0 = 5mA$ to	1.0A			8.0	
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$			-1.0		mV/°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to 1 T <sub>A</sub> =+25 °C	00KHz		10		μV/V <sub>O</sub>
Ripple Rejection	RR	f = 120Hz, I <sub>O</sub> = 500mA V <sub>I</sub> = 18.5V to 28.5V			57		dB
Dropout Voltage	$V_D$	I <sub>O</sub> = 1A, T <sub>J</sub> =+25 °C			2.0		V
Output Resistance	Ro	f = 1KHz			19		mΩ
Short Circuit Current	Isc	V <sub>I</sub> = 35V, T <sub>A</sub>	=+25 °C		250		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+25 °C	·		2.2		Α

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant, junction temperature. Change in  $V_{\text{O}}$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.



### LM7824A/RA ELECTRICAL CHARACTERISTICS

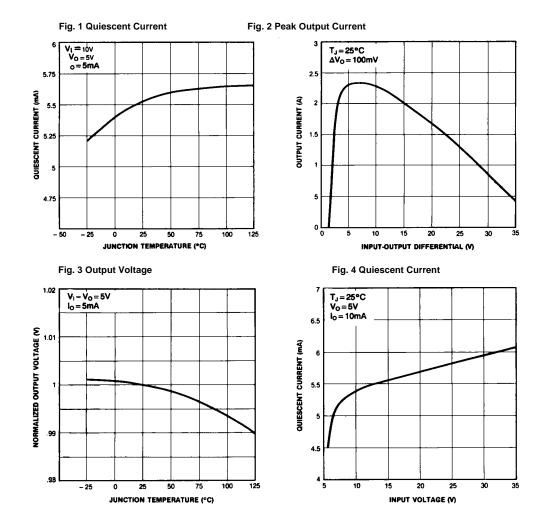
(Refer to the test circuits.  $T_J = 0$  to +150 °C,  $I_O = 1A$ ,  $V_I = 33V$ ,  $C_I = 0.33\mu F$ ,  $C_O = 0.1\mu F$ , unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> =+25 °C	23.5	24	24.5	
Output Voltage	Vo	$I_{O} = 5mA \text{ to } 1A, P_{D} \le 15W$ $V_{I} = 27.3 \text{ to } 38V$	23	24	25	V
		V <sub>I</sub> = 27 to 38V I <sub>O</sub> = 500mA		18	240	
Line Regulation	$\Delta V_{O}$	V <sub>I</sub> = 21 to 33V		6	240	mV
		T <sub>.I</sub> =+25 °C V <sub>I</sub> = 26.7V to 38V		18	240	
		V <sub>I</sub> = 30V to 36V		6	120	
Load Regulation	ΔVο	$T_J$ =+25 °C $I_O$ = 5mA to 1.5A		15	100	mV
Load Regulation	Δνο	I <sub>O</sub> = 5mA to 1.0A		15	100	IIIV
		I <sub>O</sub> = 250 to 750mA		7	50	
Quiescent Current	ΙQ	T <sub>J</sub> =+25 °C		5.2	6.0	mA
		$V_1 = 27.3V \text{ to } 38V, T_J = +25 ^{\circ}\text{C}$			0.5	
Quiescent Current Change	$\Delta I_{Q}$	$V_1 = 27.3V$ to 38V, $I_0 = 500$ mA			0.8	mA
		$I_O = 5mA$ to 1.0A			0.8	
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$		-1.5		mV/°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to 100KHz T <sub>A</sub> = 25 °C		10		μV/V <sub>O</sub>
Ripple Rejection	RR	f = 120Hz, I <sub>O</sub> = 500mA V <sub>I</sub> = 18.5V to 28.5V		54		dB
Dropout Voltage	V <sub>D</sub>	I <sub>O</sub> = 1A, T <sub>J</sub> =+25°C		2.0		V
Output Resistance	Ro	f = 1KHz		20		mΩ
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = 35V, T <sub>A</sub> =+25 °C		250		mA
Peak Current	$I_{PK}$	T <sub>J</sub> =+25 °C		2.2		Α

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant, junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.



### **TYPICAL PERFORMANCE CHARACTERISTICS**





### **TYPICAL APPLICATIONS**

Fig. 5 DC Parameters

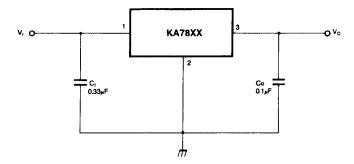


Fig. 6 Load Regulation

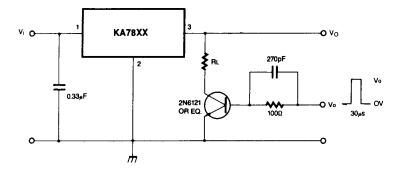


Fig. 7 Ripple Rejection

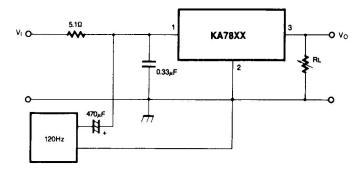
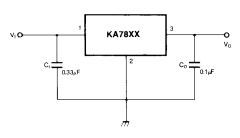
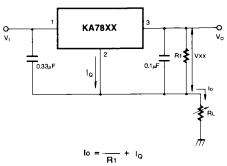




Fig. 8 Fixed Output Regulator

Fig. 9 Constant Current Regulator





### Notes:

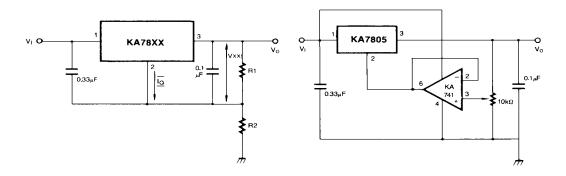
- (1) To specify an output voltage. substitute voltage value for "XX."

  A common ground is required between the input and the Output voltage. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.

  (2) C<sub>1</sub> is required if regulator is located an appreciable distance from
- power Supply filter.
  (3) Co improves stability and transient response.

Fig. 10 Circuit for Increasing Output Voltage

Fig. 11 Adjustable Output Regulator (7 to 30V)

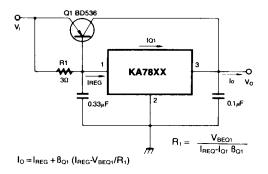


$$I_{RI} \ge 5 I_{Q}$$
  
 $V_{O} = V_{XX} (1+R_{2}/R_{1})+I_{Q}R_{2}$ 



### **TYPICAL APPLICATIONS (Continued)**

Fig. 12 High Current Voltage Regulator Fig. 13 High Output Current with Short Circuit Protection



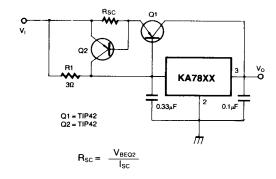
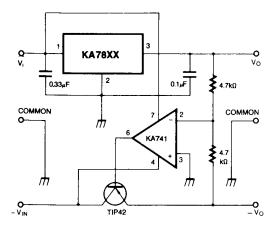
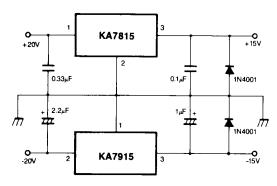


Fig. 14 Tracking Voltage Regulator

Fig. 15 Split Power Supply (±15V-1A)



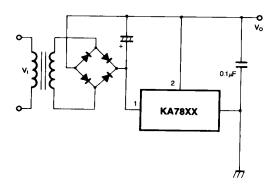


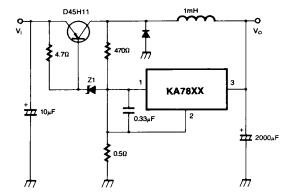


# **TYPICAL APPLICATIONS** (Continued)

Fig. 16 Negative Output Voltage Circuit

Fig. 17 switching Regulator









### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

### **PRODUCT STATUS DEFINITIONS**

### **Definition of Terms**

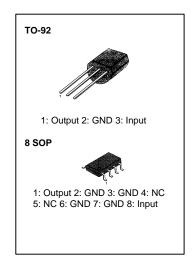
Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

### **3-TERMINAL 0.1A POSITIVE VOLTAGE REGULATORS**

The LM78LXX series of fixed voltage monolithic integrated circuit voltage regulators are suitable for application that required supply

### **FEATURES**

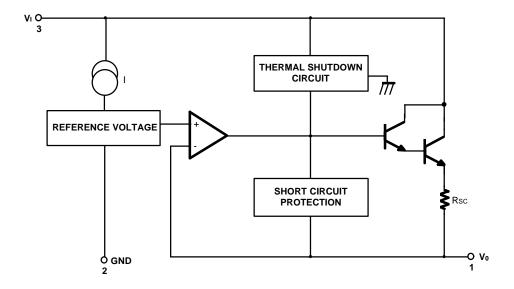
- Maximum Output Current of 100mA
  Output Voltage of 5V, 6V, 8V, 9V, 10V, 12V, 15V, 18V and 24V
- Thermal Overload Protection
- Short Circuit Current Limiting
- Output Voltage Offered in ± 5% Tolerance



### **ORDERING INFORMATION**

Device	Package	Operating Temperature
LM78LXXACZ	TO-92	- 45 ~ + 125°C °
LM78LXXM	8 SOP	0 ~ + 125°C

### **BLOCK DIAGRAM**





### **ABSOLUTE MAXIMUM RATINGS** ( $T_A = 25 \,^{\circ}\text{C}$ , unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage (for V <sub>O</sub> = 5V, 8V)	V <sub>I</sub>	30	V
(for $V_0 = 12V, 15V$ )		35	V
Operating Junction Temperature Range	$T_J$	0 ~ +150	°C
Storage Temperature Range	T <sub>STG</sub>	-65 ~ +150	°C

### LM78L05 ELECTRICAL CHARACTERISTICS

 $(V_I=10V,\,I_O=40mA,\,0\,^{\circ}C\leq T_J\leq 125\,^{\circ}C,\,C_I=0.33\,\mu F,\,C_O=0.1\mu F,\,unless\,otherwise\,specified.\,(Note\,1)$ 

Characte	Characteristic		Test	Conditions	Min	Тур	Max	Unit
Output Voltage		Vo	T <sub>J</sub> = 25 °C		4.8	5.0	5.2	V
Line Demulation	ine Regulation			$7V \le V_I \le 20V$		8	150	mV
Line Regulation		$\Delta V_{O}$	T <sub>J</sub> = 25°C	$8V \le V_i \le 20V$		6	100	mV
		$\Delta V_{\Omega}$	T 05.00	$1mA \le I_O \le 100mA$		11	60	mV
Load Regulation	Load Regulation		$T_J = 25$ °C	$1mA \leq I_O \leq 40mA$		5.0	30	mV
			$7V \le V_1 \le 0V$	$1mA \le I_0 \le 40mA$			5.25	V
Output Voltage	Output Voltage		7V ≤V <sub>I</sub> ≤ V <sub>MAX</sub> (Note 2)	$1mA \le I_0 \le 70mA$	4.75		5.25	V
Quiescent Current		ΙQ	T <sub>J</sub> = 25°C			2.0	5.5	mA
Quiescent Current	with line	$\Delta I_Q$	$8V \le V_1 \le 20V$				1.5	mA
Change	with load	$\Delta I_Q$	$1 \text{mA} \le I_0 \le 40 \text{ m}$	A			0.1	mA
Output Noise Voltage	е	V <sub>N</sub>	T <sub>A</sub> = 25 °C, 10H	z ≤ f ≤ 100KHz		40		μV/V <sub>O</sub>
Temperature Coefficient of V <sub>O</sub>		ΔV <sub>O</sub> /ΔΤ	I <sub>O</sub> = 5mA			-0.65		mV/°C
Ripple Rejection		RR	$f = 120Hz, 8V \le V_1 \le 18V, T_J = 25^{\circ}C$		41	80		dB
Dropout Voltage		$V_D$	T <sub>J</sub> = 25 °C			1.7		V



### LM78L06 ELECTRICAL CHARACTERISTICS

 $(V_I=12V,\,I_O=40mA,\,0\,^{\circ}C\leq T_J\leq 125\,^{\circ}C\,\,,\,C_I=0.33\mu F,\,C_O=0.1\mu F,\,unless\,\,otherwise\,\,specified.\,\,(Note\,\,1)$ 

Characteri	stic	Symbol	Т	Test Conditions		Тур	Max	Unit
Output Voltage		Vo	T <sub>J</sub> = 25 °C		5.75	6.0	6.25	V
Line Demulation				8.5V < V <sub>I</sub> < 20V		64	175	mV
Line Regulation		$\Delta V_{O}$	T <sub>J</sub> =25 °C	$9V \ge V_1 \ge 20V$		54	125	mV
		41/	T 07:0	1mA < I <sub>O</sub> < 100mA		12.8	80	mV
Load Regulation		$\Delta V_{O}$	T <sub>J</sub> =25 °C	1mA < I <sub>O</sub> < 70mA		5.8	40	mV
Output Voltage		Vo	8.5 < V <sub>I</sub> < 20V, 1mA < I <sub>O</sub> < 40mA		5.7		6.3	
Output voltage	Output Voltage		8.5 < $V_1$ < $V_{MAX}$ (Note), 1mA < $I_0$ < 70mA		5.7		6.3	V
			$T_J = 25 ^{\circ}\text{C}$			3.9	6.0	mA
Quiescent Current		lα	T <sub>J</sub> = 125 °C				5.5	IIIA
Quiescent Current	with line	$\Delta I_Q$	$9 < V_1 < 20V$				1.5	
Change	with load	$\Delta I_Q$	1mA < I <sub>O</sub> < 40n	nA			0.1	mA
Output Noise Voltage	е	V <sub>N</sub>	T <sub>A</sub> = 25 °C, 10	Hz < f < 100KHz		40		μV/V <sub>O</sub>
Temperature Coeffic	ient of V <sub>O</sub>	ΔV <sub>O</sub> /ΔΤ	$I_O = 5mA$			0.75		mV/°C
Ripple Rejection		RR	f = 120Hz, 10V < V <sub>I</sub> < 20V, T <sub>J</sub> = 25 °C		40	46		dB
Dropout Voltage		$V_D$	T <sub>J</sub> = 25 °C			1.7		V

### LM78L08 ELECTRICAL CHARACTERISTICS

 $(V_I=14V,~I_O=40mA,~0~^{\circ}C \leq T_J \leq 125~^{\circ}C,~C_I=0.33~\mu F,~C_O=0.1\mu F,~unless~otherwise~specified.~(Note~1)$ 

Characteri	stic	Symbol	Test	Conditions	Min	Тур	Max	Unit
Output Voltage		Vo	T <sub>J</sub> = 25 °C		7.7	8.0	8.3	V
Line De sudeties				$10.5V \le V_1 \le 23V$		10	175	mV
Line Regulation		$\Delta V_{O}$	T <sub>J</sub> =25 °C	$11V \le V_1 \le 23V$		8	125	mV
			T 0500	$1mA \le I_0 \le 100mA$		15	80	mV
Load Regulation	Load Regulation		T <sub>J</sub> =25 °C	$1mA \le I_0 \le 40mA$		8.0	40	mV
			$10.5 V \leq V_I \leq 23 V$	$1mA \le I_0 \le 40mA$	7.6		8.4	V
Output Voltage	Output Voltage		$10.5V \le V_1 \le V_{MAX}$ (Note 2)	$1mA \le I_0 \le 70mA$	7.6		8.4	V
Quiescent Current		lα	T <sub>J</sub> = 25 °C			2.0	5.5	mA
Quiescent Current	with line	$\Delta I_Q$	$11V \le V_1 \le 23V$				1.5	mA
Change	with load	$\Delta I_Q$	$1mA \le I_O \le 40mA$				0.1	mA
Output Noise Voltag	e	V <sub>N</sub>	T <sub>A</sub> = 25 °C, 10Hz ≤	f ≤100KHz		60		μV/V <sub>O</sub>
Temperature Coefficient of Vo		$\Delta V_{O}/\Delta T$	I <sub>O</sub> = 5mA			-0.8		mV/°C
Ripple Rejection		RR	f = 120Hz, 11V ≤ V	≤ 21V, T <sub>J</sub> = 25°C	39	70		dB
Dropout Voltage		$V_D$	T <sub>J</sub> = 25 °C			1.7		V



### LM78L09 ELECTRICAL CHARACTERISTICS

 $(V_I = 15V, I_O = 40mA, 0 \degree C \le T_J \le 125 \degree C, C_I = 0.33 \ \mu F, C_O = 0.1 \mu F, unless otherwise specified. (Note 1)$ 

Characteri	stic	Symbol	Test	Conditions	Min	Тур	Max	Unit
Output Voltage		Vo	T <sub>J</sub> = 25 °C		8.64	9.0	9.36	V
				$11.5 \text{V} \leq \text{V}_{\text{I}} \leq 24 \text{V}$		90	200	mV
Line Regulation		$\Delta V_{O}$	T <sub>J</sub> =25°C	$13V \leq V_I \leq 24V$		100	150	mV
			T 05:00	$1mA \le I_0 \le 100mA$		20	90	mV
Load Regulation		$\Delta V_{O}$	T <sub>J</sub> =25 °C	$1mA \leq I_O \leq 40mA$		10	45	mV
			$11.5 \text{V} \leq \text{V}_{\text{I}} \leq 24 \text{V}$	$1mA \leq I_O \leq 40mA$	8.55		9.45	V
Output Voltage		Vo	$11.5V \le V_{I} \le V_{MAX}$ (Note 2)	$1mA \le I_0 \le 70mA$	8.55		9.45	V
Quiescent Current		lα	T <sub>J</sub> = 25 °C			2.1	6.0	mA
Quiescent Current	with line	$\Delta I_Q$	$13V \le V_1 \le 24V$				1.5	mA
Change	with load	$\Delta I_Q$	$1mA \le I_0 \le 40mA$				0.1	mA
Output Noise Voltage	е	V <sub>N</sub>	$T_A = 25 ^{\circ}C$ , $10Hz \leq$	f ≤ 100KHz		70		$\mu V/V_O$
Temperature Coefficient of Vo		ΔV <sub>O</sub> /ΔΤ	I <sub>O</sub> = 5mA			-0.9		mV/°C
Ripple Rejection		RR	$f = 120Hz, 12V \le V_1 \le 22V, T_J = 25 \degree C$		38	44		dB
Dropout Voltage		$V_D$	T <sub>J</sub> = 25 °C			1.7		V

### LM78L10 ELECTRICAL CHARACTERISTICS

 $(V_1 = 16V, I_O = 40mA, 0 \degree C < T_J < 125 \degree C, C_1 = 0.33 \ \mu F, C_O = 0.1 \mu F, unless otherwise specified. (Note 1)$ 

Characteris	tic	Symbol	Т	est Conditions	Min	Тур	Max	Unit
Output Voltage		Vo	T <sub>J</sub> = 25 °C		9.6	10.0	10.4	V
Line Description	II B 12			12.5 < V <sub>I</sub> < 25V		100	220	mV
Line Regulation		$\Delta V_{O}$	T <sub>J</sub> =25 °C	$14V \geq V_I \geq 25V$		100	170	mV
		41/	T 0500	1mA < I <sub>O</sub> < 100mA		20	94	mV
Load Regulation	ulation $\Delta V_0 = T_J = 25 ^{\circ}\text{C}$ $1\text{mA} < I_0 < 70\text{mA}$			10	47	mV		
Output Valtage		Vo	$12.5 < V_1 < 25V$	2.5 < V <sub>I</sub> < 25V, 1mA < I <sub>O</sub> < 40mA			10.5	
Output Voltage		12.5 $< V_1 < V_{MAX}(Note)$ , 1mA $< I_0 < 70$ mA		9.5		10.5	V	
			T <sub>J</sub> = 25 °C			4.2	6.5	A
Quiescent Current		lα	T <sub>J</sub> = 125 °C				6.0	mA
Quiescent Current	with line	$\Delta I_Q$	12.5 < V <sub>I</sub> < 25V				1.5	mA
Change	with load	$\Delta I_Q$	1mA < I <sub>0</sub> < 40m	nA			0.1	IIIA
Output Noise Voltage	е	$V_N$	T <sub>A</sub> = 25 °C, 10H	lz < f < 100KHz		74		μV/V <sub>O</sub>
Temperature Coeffic	eient of Vo	$\Delta V_{O}/\Delta T$	I <sub>O</sub> = 5mA			0.95		mV/°C
Ripple Rejection		RR	f = 120Hz, 15V < V <sub>I</sub> < 25V, T <sub>J</sub> = 25 °C		38	43		dB
Dropout Voltage		V <sub>D</sub>	T <sub>J</sub> = 25 °C			1.7		V



### LM78L12 ELECTRICAL CHARACTERISTICS

 $(V_I = 19V, I_O = 40mA, 0 \degree C \le T_J \le 125 \degree C, C_I = 0.33 \ \mu F, C_O = 0.1 \mu F, unless otherwise specified. (Note 1)$ 

Characteri	Characteristic		Test	Conditions	Min	Тур	Max	Unit
Output Voltage		Vo	T <sub>J</sub> = 25 °C		11.5	12	12.5	V
Line Demulation				$14.5 \text{V} \leq \text{V}_{\text{I}} \leq 27 \text{V}$		20	250	mV
Line Regulation		$\Delta V_{O}$	T <sub>J</sub> =25°C	$16V \le V_1 \le 27V$		15	200	mV
			T 0500	$1mA \le I_0 \le 100mA$		20	100	mV
Load Regulation		$\Delta V_{O}$	T <sub>J</sub> =25 °C	$1mA \le I_0 \le 40mA$		10	50	mV
			$14.5 \text{V} \leq \text{V}_{\text{I}} \leq 27 \text{V}$	$1mA \le I_0 \le 40mA$	11.4		12.6	V
Output Voltage		Vo	$14.5V \le V_I \le V_{MAX}$ (Note 2)	$1mA \le I_0 \le 70mA$	11.4		12.6	٧
Quiescent Current		ΙQ	T <sub>J</sub> = 25 °C			2.1	6.0	mA
Quiescent Current	with line	$\Delta I_Q$	$16V \le V_1 \le 27V$				1.5	mA
Change	with load	$\Delta I_Q$	$1mA \le I_O \le 40mA$				0.1	mA
Output Noise Voltage	е	$V_N$	T <sub>A</sub> = 25 °C, 10Hz ≤	f ≤ 100KHz		80		$\mu V/V_O$
Temperature Coefficient of V <sub>O</sub>		ΔV <sub>O</sub> /ΔΤ	I <sub>O</sub> = 5mA			-1.0		mV/°C
Ripple Rejection		RR	$f = 120Hz, 15V \le V_1 \le 25V, T_J = 25 ^{\circ}C$		37	65		dB
Dropout Voltage		$V_D$	T <sub>J</sub> = 25 °C			1.7		V

### LM78L15 ELECTRICAL CHARACTERISTICS

 $(V_1 = 23V, I_O = 40mA, 0 \degree C \le T_J \le 125 \degree C, C_1 = 0.33 \ \mu F, C_O = 0.1 \mu F, unless otherwise specified. (Note 1)$ 

Characteri	stic	Symbol	Test	Conditions	Min	Тур	Max	Unit
Output Voltage		Vo	T <sub>J</sub> = 25 °C		14.4	15	15.6	V
Line Demoleties				$17.5V \le V_1 \le 30V$		25	300	mV
Line Regulation		$\Delta V_{O}$	T <sub>J</sub> =25 °C	$20V \le V_1 \le 30V$		20	250	mV
			T 05.00	$1mA \le I_O \le 100mA$		25	150	mV
Load Regulation		$\Delta V_{O}$	T <sub>J</sub> =25 °C	$1mA \le I_O \le 40mA$		12	75	mV
			$17.5 \text{V} \leq \text{V}_{\text{I}} \leq 30 \text{V}$	$1mA \le I_O \le 40mA$	14.25		15.75	V
Output Voltage		Vo	$17.5V \le V_{I} \le V_{MAX}$ (Note 2)	1mA ≤ I <sub>O</sub> ≤ 70mA	14.25		15.75	٧
Quiescent Current		ΙQ	T <sub>J</sub> = 25 °C			2.1	6.0	mA
Quiescent Current	with line	$\Delta I_Q$	$20V \leq V_I \leq 30V$				1.5	mA
Change	with load	$\Delta I_Q$	$1mA \le I_0 \le 40mA$				0.1	mA
Output Noise Voltage	е	V <sub>N</sub>	T <sub>A</sub> = 25 °C, 10Hz ≤	f ≤ 100KHz		90		μV/V <sub>O</sub>
Temperature Coeffic	eient of Vo	ΔV <sub>O</sub> /ΔΤ	I <sub>O</sub> = 5mA			-1.3		mV/°C
Ripple Rejection		RR $f = 120$ Hz, $18.5$ V $\leq V_{I} \leq 28.5$ V, $T_{J} = 25$ °C		34	60		dB	
Dropout Voltage		$V_D$	T <sub>J</sub> = 25 °C			1.7		V



### LM78L18 ELECTRICAL CHARACTERISTICS

 $(V_1 = 27V, I_O = 40mA, 0 \degree C \le T_J \le 125 \degree C, C_1 = 0.33 \ \mu F, C_O = 0.1 \mu F, unless otherwise specified. (Note 1)$ 

Characteri	Characteristic		Test	t Conditions	Min	Тур	Max	Unit
Output Voltage		Vo	T <sub>J</sub> = 25 °C		17.3	18	18.7	V
Line Degulation				$21 V \leq V_I \leq 33 V$		145	300	mV
Line Regulation		$\Delta V_{O}$	T <sub>J</sub> =25 °C	$22V \leq V_I \leq 33V$		135	250	mV
			T 0500	$1mA \le I_0 \le 100mA$		30	170	mV
Load Regulation		$\Delta V_{O}$	T <sub>J</sub> =25 °C	$1mA \leq I_O \leq 40mA$		15	85	mV
			$21V \le V_1 \le 33V$	$1mA \le I_O \le 40mA$	17.1		18.9	V
Output Voltage		Vo	21V ≤ V <sub>I</sub> ≤ V <sub>MAX</sub> (Note 2)	$1mA \le I_O \le 70mA$	17.1		18.9	V
Quiescent Current		ΙQ	T <sub>J</sub> = 25 °C			2.2	6.0	mA
Quiescent Current	with line	$\Delta I_Q$	$21V \le V_1 \le 33V$				1.5	mA
Change	with load	$\Delta I_Q$	$1mA \le I_O \le 40mA$				0.1	mA
Output Noise Voltage	e	V <sub>N</sub>	T <sub>A</sub> = 25 °C, 10Hz ≤	≤ f ≤ 100KHz		150		μV/V <sub>O</sub>
Temperature Coefficient of V <sub>O</sub>		ΔV <sub>O</sub> /ΔΤ	I <sub>O</sub> = 5mA			-1.8		mV/°C
Ripple Rejection RR $f = 120$ Hz, $23$ V $\leq$ V <sub>I</sub> $\leq$ $33$ V, T <sub>J</sub> $= 25$ $^{\circ}$ C		V <sub>I</sub> ≤ 33V, T <sub>J</sub> = 25 °C	34	48		dB		
Dropout Voltage		$V_D$	T <sub>J</sub> = 25 °C			1.7		V

### LM78L24 ELECTRICAL CHARACTERISTICS

 $(V_I=33V,\,I_O=40mA,\,0\,^{\circ}C\leq T_J\leq 125\,^{\circ}C,\,C_I=0.33~\mu F,\,C_O=0.1\mu F,\,unless~otherwise~specified.~(Note~1)$ 

Characteri	Characteristic		Test Conditions		Min	Тур	Max	Unit
Output Voltage		Vo	T <sub>J</sub> = 25 °C		23	24	25	V
5				$27V \le V_1 \le 38V$		160	300	mV
Line Regulation		$\Delta V_{O}$	T <sub>J</sub> =25 °C	$28V \le V_1 \le 38V$		150	250	mV
			T 07:0	$1mA \le I_0 \le 100mA$		40	200	mV
Load Regulation		$\Delta V_{O}$	T <sub>J</sub> =25 °C	$1mA \le I_0 \le 40mA$		20	100	mV
			$27V \le V_1 \le 38V$	$1mA \le I_0 \le 40mA$	22.8		25.2	V
Output Voltage		Vo	$27V \le V_1 \le V_{MAX}$ (Note 2)	1mA ≤ I <sub>O</sub> ≤ 70mA	22.8		25.2	٧
Quiescent Current		ΙQ	T <sub>J</sub> = 25°C			2.2	6.0	mA
Quiescent Current	with line	$\Delta I_Q$	$28V \le V_1 \le 38V$				1.5	mA
Change	with load	$\Delta I_Q$	$1mA \le I_0 \le 40mA$				0.1	mA
Output Noise Voltag	е	$V_N$	T <sub>A</sub> = 25 °C, 10Hz s	≤ f ≤ 100KHz		200		μV/V <sub>O</sub>
Temperature Coefficient of Vo		ΔV <sub>O</sub> /ΔΤ	I <sub>O</sub> = 5mA			-2.0		mV/°C
Ripple Rejection		RR	f = 120Hz, 28V ≤ V₁ ≤ 38V, T₁ = 25°C		34	45		dB
Dropout Voltage		$V_D$	T <sub>J</sub> = 25 °C			1.7		V

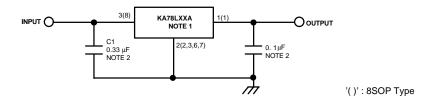
### Notes



<sup>1.</sup> The maximum steady state usable output current and input voltage are very dependent on the heat sinking and/or lead length of the package. The data above represent pulse test conditions with junction temperature as indicated at the initiation of tests.

<sup>2.</sup> Power dissipation ≤ 0.75W.

### **TYPICAL APPLICATION**



### Notes

- To specify an output voltage, substitute voltage value for "XX".
   Bypass Capacitors are recommend for optimum stability and transient response and should be located as close as



### **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

### **PRODUCT STATUS DEFINITIONS**

### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.



# MC78MXX (LM78MXX) (KA78MXX)

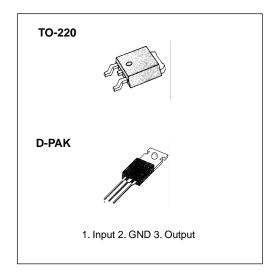
# 3-Terminal 0.5A Positive Voltage Regulators

### **Features**

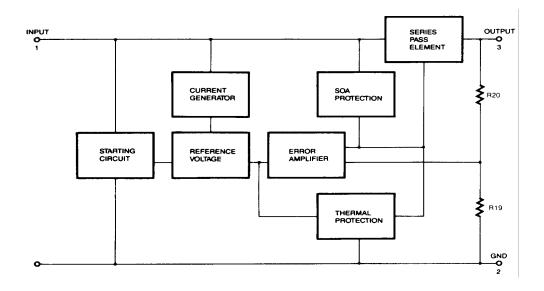
- Output Current up to 0.5A
- Output Voltages of 5, 6, 8, 10, 12, 15, 18, 20, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor SOA Protection
- · Industrial and commercial temperature range

# **Description**

The MC78MXX (LM78MXX) (KA78MXX) series of three-terminal positive regulators are available in the TO-220/D-PAK package with several fixed output voltages making it useful in a wide range of applications.



# **Internal Block Diagram**



# Absolute Maximum Ratings (Ta=+25°C, Unless otherwise specified)

Parameter	Symbol	Value	Unit
Input Voltage (for V <sub>O</sub> = 5V to 18V)	VI	35	V
(for V <sub>O</sub> = 24V)	VI	40	V
Thermal Resistance Junction-Cases	R <sub>0</sub> JC	5	°C/W
Thermal Resistance Junction-Air	RθJA	65	°C/W
Operating Temperature Range KA78MXXI/RI	TOPR	-40~ + 125	°C
KA78MXX/R		0~ + 125	°C
Storage Temperature Range	TSTG	-65~ + 150	°C

# KA78M05/I/R/RI Electrical Characteristics

(Refer to the test circuits,  $T_{MIN} \le T_J \le +125$ °C,  $I_O=350$ mA,  $V_I=10$ V, unless otherwise specified,  $C_I=0.33$ mF,  $C_O=0.1$ mF)

Parameter	Symbol	Con	ditions	Min.	Тур.	Max.	Units
Output Voltage	Vo	T <sub>J</sub> =+25°C		4.8	5	5.2	V
		IO = 5 to 350m V <sub>I</sub> = 7 to 20V	IO = 5 to 350mA VI= 7 to 20V		5	5.25	
Line Regulation	ΔVO	I <sub>O</sub> = 200mA	V <sub>I</sub> = 7 to 25V	-	-	100	mV
		TJ =+25°C	V <sub>I</sub> = 8 to 25V	-	-	50	
Load Regulation	ΔVO	IO = 5mA to 0.	5A, TJ =+25°C	-	-	100	mV
		I <sub>O</sub> = 5mA to 20	00mA, TJ =+25 °C	-	-	50	
Quiescent Current	IQ	TJ=+25°C		-	4.0	6	mA
Quiescent Current	ΔlQ	IO = 5mA to 35	50mA	-	-	0.5	mA
Change		IO = 200mA VI = 8 to 25V		-	-	0.8	
Output Voltage Drift	ΔV/ΔΤ	IO = 5mA T <sub>J</sub> = 0 to +125	°C	-	- 0.5	-	mV/°C
Output Noise Voltage	VN	f = 10Hz to 100	OKHz	-	40	-	mV/Vo
Ripple Rejection	RR	f = 120Hz, I <sub>O</sub> = 300mA V <sub>I</sub> = 8 to 18V		62	-	-	dB
Dropout Voltage	VD	T <sub>J</sub> =+25°C, I <sub>O</sub> = 500mA		-	2	-	V
Short Circuit Current	Isc	TJ=+25°C, VI=	: 35V	-	300	-	mA
Peak Current	IPK	T <sub>J</sub> =+25°C		-	700	-	mA

### NOTE:

1. TMIN<TJ<TMAX

KA78MXX/RI:  $T_{MIN}$ = -40°C,  $T_{MAX}$  = +125°C KA78MXX/R:  $T_{MIN}$ = 0°C,  $T_{MAX}$  = +125°C

# KA78M06/I/R/RI Electrical Characteristics

 $(Refer \ to \ the \ test \ circuits, T_{MIN} \leq T_{J} \leq +125^{\circ}C, \ I_{O} = 350 mA, \ V_{I} = 11V, \ unless \ otherwise \ specified, \ C_{I} = 0.33 mF, \ C_{O} = 0.1 mF) (C_{O} = 0.1 mF) (C_{$ 

Parameter	Symbol	Conditions		Min.	Тур.	Max.	Units
Output Voltage	Vo	TJ=+25°C I <sub>O</sub> = 5 to 350mA V <sub>I</sub> = 8 to 21V		5.75	6	6.25	V
				5.7	6	6.3	
Line Regulation	ΔVO	I <sub>O</sub> = 200mA	V <sub>I</sub> = 8 to 25V	-	-	100	mV
		TJ =+25°C	VI = 9 to 25V	-	-	50	
Load Regulation	ΔVO	$I_O = 5mA$ to (	).5A, T <sub>J</sub> =+25°C	-	-	120	mV
		IO = 5mA to 2	200mA, TJ =+25°C	-	-	60	
Quiescent Current	IQ	T <sub>J</sub> =+25°C		-	4.0	6	mA
Quiescent Current Change	ΔlQ	I <sub>O</sub> = 5mA to 350mA I <sub>O</sub> = 200mA V <sub>I</sub> = 9 to 25V		-	-	0.5	mA
				-	-	0.8	
Output Voltage Drift	ΔV/ΔΤ	I <sub>O</sub> = 5mA T <sub>J</sub> = 0 to +125°C		-	- 0.5	-	mV/°C
Output Noise Voltage	VN	f = 10Hz to 10	00KHz	-	45	-	mV/VO
Ripple Rejection	RR	f = 120Hz, I <sub>O</sub> = 300mA V <sub>I</sub> = 9 to 19V		59	-	-	dB
Dropout Voltage	VD	T <sub>J</sub> =+25°C, I <sub>O</sub> = 500mA		-	2	-	V
Short Circuit Current	Isc	TJ= +25°C, V	'ı= 35V	-	300	-	mA
Peak Current	IPK	TJ =+25°C		-	700	-	mA

### NOTE:

1. TMIN:

KA78MXX/RI:  $T_{MIN} = -40$ °C KA78MXX/R:  $T_{MIN} = 0$ °C

# Fixed Voltage Regulator (Positive)

# KA78M08/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to the test circuits,  $T_{MIN} \le T_J \le +125$ °C,  $I_O = 350$ mA,  $V_I = 14$ V, unless otherwise specified,  $C_I = 0.33$ mF,  $C_O = 0.1$ mF)

Parameter	Symbol	Conditions		Min.	Тур.	Max.	Units
Output Voltage	Vo	TJ=+25 °C		7.7	8	8.3	V
		I <sub>O</sub> = 5 to 350mA V <sub>I</sub> = 10.5 to 23V		7.6	8	8.4	
Line Regulation	ΔVο	I <sub>O</sub> = 200mA	V <sub>I</sub> = 10.5 to 25V	-	-	100	mV
	TJ	TJ =+25°C	V <sub>I</sub> = 11 to 25V	-	-	50	1
Load Regulation	ΔVO	$I_O = 5mA$ to $C$	).5A, T <sub>J</sub> =+25°C	-	-	160	mV
		IO = 5mA to 2	200mA, TJ =+25°C	-	-	80	1
Quiescent Current	IQ	T <sub>J=+25°</sub> C		-	4.0	6	mA
Quiescent Current Change	ΔlQ	I <sub>O</sub> = 5mA to 350mA I <sub>O</sub> = 200mA V <sub>I</sub> = 10.5 to 25V		-	-	0.5	mA
				-	-	0.8	
Output Voltage Drift	RR	I <sub>O</sub> = 5mA T <sub>J</sub> = 0 to +125°C		-	- 0.5	-	mV/°C
Output Noise Voltage	VN	f = 10Hz to 10	00KHz	-	52	-	mV/VO
Ripple Rejection	RR	f = 120Hz, IO = 300mA VI = 9 to 19V		56	-	-	dB
Dropout Voltage	VD	TJ =+25°C,IO = 500mA		-	2	-	V
Short Circuit Current	Isc	TJ =+25°C, V	i= 35V	-	300	-	mA
Peak Current	IPK	TJ =+25°C		-	700	-	mA

### NOTE:

1. TMIN:

KA78MXX/RI:  $T_{MIN} = -40$ °C KA78MXX/R:  $T_{MIN} = 0$ °C

# KA78M10/I/R/RI Electrical Characteristics

(Refer to the test circuits,  $T_{MIN} \le T_J \le +125$ °C,  $I_O = 350$ mA,  $V_I = 17$ V, unless otherwise specified,  $C_I = 0.33$ mF,  $C_O = 0.1$ mF)

Parameter	Symbol	Conditions		Min.	Тур.	Max.	Units
Output Voltage	Vo	TJ= +25°C		9.6	10	10.4	V
		I <sub>O</sub> = 5 to 350mA V <sub>I</sub> = 12.5 to 25V		9.5	10	10.5	
Line Regulation	ΔVο	I <sub>O</sub> = 200mA	V <sub>I</sub> = 12.5 to 25V	-	-	100	mV
		TJ =+25°C	V <sub>I</sub> = 13 to 25V	-	-	50	1
Load Regulation	ΔVο	$I_O = 5mA \text{ to } C$	).5A, T <sub>J</sub> =+25°C	-	-	200	mV
		IO = 5mA to 2	200mA, TJ =+25°C	-	-	100	
Quiescent Current	IQ	TJ=+25°C	T <sub>J</sub> =+25°C		4.1	6	mA
Quiescent Current Change	ΔlQ	I <sub>O</sub> = 5mA to 350mA I <sub>O</sub> = 200mA V <sub>I</sub> = 12.5 to 25V		-	-	0.5	mA
				-	-	0.8	
Output Voltage Drift	ΔV/ΔΤ	I <sub>O</sub> = 5mA T <sub>J</sub> = 0 to +125°C		-	- 0.5	-	mV/°C
Output Noise Voltage	VN	f = 10Hz to 10	00KHz	-	65	-	mV/VO
Ripple Rejection	RR	f = 120Hz, IO = 300mA VI = 13 to 23V		55	-	-	dB
Dropout Voltage	VD	T <sub>J</sub> =+25°C, I <sub>O</sub> = 500mA		-	2	-	V
Short Circuit Current	Isc	T <sub>J</sub> = +25°C, V	i= 35V	-	300	-	mA
Peak Current	IPK	TJ =+25°C		-	700	-	mA

### NOTE:

1. TMIN:

KA78MXX/RI:  $T_{MIN} = -40$ °C KA78MXX/R:  $T_{MIN} = 0$ °C

# KA78M12/I/R/RI Electrical Characteristics

(Refer to the test circuits,  $T_{MIN} \le T_J \le 125$ °C,  $I_O = 350$ mA,  $V_I = 19$ V, unless otherwise specified,  $C_I = 0.33$ mF,  $C_O = 0.1$ mF)

Parameter	Symbol	Cor	nditions	Min.	Тур.	Max.	Units
Output Voltage	Vo	TJ=+25°C I <sub>O</sub> = 5 to 350mA V <sub>I</sub> = 14.5 to 27V		11.5	12	12.5	V
				11.5	12	12.6	
Line Regulation	ΔVO	I <sub>O</sub> = 200mA	V <sub>I</sub> = 14.5 to 30V	-	-	100	mV
		TJ =+25°C	VI = 16 to 30V	-	-	50	
Load Regulation	$\Delta V^{O}$	$I_O = 5mA$ to (	).5A, T <sub>J</sub> =+25°C	-	-	240	mV
		IO = 5mA to 2	200mA, TJ =+25°C	-	-	120	
Quiescent Current	IQ	T <sub>J</sub> =+25°C		-	4.1	6	mA
Quiescent Current Change	ΔlQ	I <sub>O</sub> = 5mA to 350mA I <sub>O</sub> = 200mA V <sub>I</sub> = 14.5 to 30V		-		0.5	mA
				-	-	0.8	
Output Voltage Drift	ΔV/ΔΤ	I <sub>O</sub> = 5mA T <sub>J</sub> = 0 to +125°C		-	- 0.5	-	mV/°C
Output Noise Voltage	VN	f = 10Hz to 10	00KHz	-	75	-	mV/VO
Ripple Rejection	RR	f = 120Hz, IO = 300mA VI = 15 to 25V		55		-	dB
Dropout Voltage	VD	TJ =+25°C, IO = 500mA		-	2	-	V
Short Circuit Current	Isc	T <sub>J</sub> = +25°C, V <sub>I</sub> = 35V		-	300	-	mA
Peak Current	IPK	TJ = +25°C		-	700	_	mA

### NOTE:

1. TMIN:

KA78MXX/RI:  $T_{MIN} = -40$ °C KA78MXX/R:  $T_{MIN} = 0$ °C

# KA78M15/I/R/RI ELECTRICAL CHARACTERISTICS

(Refer to the test circuits,  $T_{MIN} \le T_J \le +125$ °C,  $I_O = 350$ mA,  $V_I = 23$ V, unless otherwise specified,  $C_I = 0.33$ mF,  $C_O = 0.1$ mF)

Parameter	Symbol	Conditions		Min.	Тур.	Max.	Units
Output Voltage	Vo	TJ=+25°C		14.4	15	15.6	V
		I <sub>O</sub> = 5 to 350mA V <sub>I</sub> = 17.5 to 30V		14.25	15	15.75	
Line Regulation	ΔVο	I <sub>O</sub> = 200mA	V <sub>I</sub> = 17.5 to 30V	-	-	100	mV
		TJ =+25°C	VI = 20 to 30V	-	-	50	
Load Regulation	ΔVο	$I_O = 5mA$ to	0.5A, T <sub>J</sub> =+25°C	-	-	300	mV
		IO = 5mA to 3	200mA, TJ =+25°C	-	-	150	
Quiescent Current	IQ	T <sub>J</sub> =+25°C		-	4.1	6	mA
Quiescent Current Change	ΔlQ	I <sub>O</sub> = 5mA to 350mA I <sub>O</sub> = 200mA V <sub>I</sub> = 17.5 to 30V		-	-	0.5	mA
				-	-	0.8	
Output Voltage Drift	ΔV/ΔΤ	I <sub>O</sub> = 5mA T <sub>J</sub> = 0 to +125°C		-	- 1	-	mV/°C
Output Noise Voltage	VN	f = 10Hz to 1	00KHz	-	100	-	mV/VO
Ripple Rejection	RR	f = 120Hz, IO = 300mA VI = 18.5 to 28.5V		54			dB
Dropout Voltage	VD	TJ =+25°C, IO = 500mA		-	2	-	V
Short Circuit Current	Isc	TJ= +25°C, \	/ <sub>I</sub> = 35V	-	300	-	mA
Peak Current	lpk	T <sub>J</sub> = + 25°C		-	700	-	mA

### NOTE:

1. TMIN:

KA78MXX/RI:  $T_{MIN} = -40$ °C KA78MXX/R:  $T_{MIN} = 0$ °C

# KA78M18/I/R/RI Electrical Characteristics

(Refer to the test circuits,  $T_{MIN} \le T_J \le +125$ °C,  $I_O = 350$ mA,  $V_I = 26$ V, unless otherwise specified,  $C_I = 0.33$ mF,  $C_O = 0.1$ mF)

Parameter	Symbol	Co	nditions	Min.	Тур.	Max.	Units
Output Voltage	Vo	TJ=+25°C		17.3	18	18.7	V
		I <sub>O</sub> = 5 to 350mA V <sub>I</sub> = 20.5 to 33V		17.1	18	18.9	
Line Regulation	ΔVO	I <sub>O</sub> = 200mA	V <sub>I</sub> = 21 to 33V	-	-	100	mV
		TJ =+25°C	VI = 24 to 33V	-	-	50	
Load Regulation	ΔVΟ	IO = 5mA to	0.5A, TJ =+25°C	-	-	360	mV
		IO = 5mA to	200mA, TJ =+25°C	-	-	180	
Quiescent Current	IQ	TJ =+25°C	T <sub>J</sub> =+25°C		4.2	6	mA
Quiescent Current Change	ΔlQ	I <sub>O</sub> = 5mA to 350mA		-	-	0.5	mA
		IO = 200mA VI = 21 to 33V		-	-	0.8	
Output Voltage Drift	ΔV/ΔΤ	I <sub>O</sub> =5mA T <sub>J</sub> =0 to 125°C		-	-1.1	-	mV/°C
Output Noise Voltage	VN	f=10Hz to 100KHz			100	-	μV/VO
Ripple Rejection	RR	f=120Hz, IO=300mA		53		-	dB
Dropout Voltage	VD	TJ =+25°C, I <sub>O</sub> =500mA		-	2	-	V
Short Circuit Current	Isc	TJ =+25°C, \	/ <sub>I</sub> =35V	-	300	-	mA
Peak Current	IPK	TJ =+25°C		-	700	-	mA

### NOTE:

1. TMIN:

KA78MXX/R:  $T_{MIN} = -40$ °C KA78MXX/R:  $T_{MIN} = 0$ °C

# KA78M20/I/R/RI Electrical Characteristics

(Refer to the test circuits,  $T_{MIN} \le T_J \le +125$ °C,  $I_O = 350$ mA,  $V_I = 29$ V, unless otherwise specified,  $C_I = 0.33$ mF,  $C_O = 0.1$ mF)

Parameter	Symbol	Conditions		Min.	Тур.	Max.	Units
Output Voltage	Vo	TJ= +25°C		19.2	20	20.8	V
		I <sub>O</sub> = 5 to 350mA V <sub>I</sub> = 23 to 35V		19	20	21	
Line Regulation	ΔVO	I <sub>O</sub> = 200mA	V <sub>I</sub> = 23 to 35V	-	-	100	mV
		TJ =+25°C	VI = 24 to 35V	-	-	50	
Load Regulation	ΔVO	IO = 5mA to	0.5A, T <sub>J</sub> =+25°C	-	-	400	mV
		IO = 5mA to	200mA, TJ =+25°C	-	-	200	
Quiescent Current	IQ	T <sub>J</sub> =+25°C		-	4.2	6	mA
Quiescent Current Change	ΔlQ	I <sub>O</sub> = 5mA to 350mA I <sub>O</sub> = 200mA V <sub>I</sub> = 23 to 35V		-	-	0.5	mA
				-	-	0.8	
Output Voltage Drift	ΔV/ΔΤ	I <sub>O</sub> = 5mA T <sub>J</sub> = 0 to +125°C		-	-1.1	-	mV/°C
Output Noise Voltage	VN	f = 10Hz to 1	00KHz	-	110	-	mV/Vo
Ripple Rejection	RR	f = 120Hz, IO = 300mA VI = 24 to 34V		53	-	-	dB
Dropout Voltage	VD	TJ =+25°C, IO = 500mA		-	2	-	V
Short Circuit Current	Isc	T <sub>J</sub> = +25°C,	V <sub>I</sub> = 35V	-	300	-	mA
Peak Current	IPK	TJ = +25°C		-	700	-	mA

### NOTE:

1. TMIN:

KA78MXX/RI:  $T_{MIN} = -40$ °C KA78MXX/R:  $T_{MIN} = 0$ °C

# KA78M24/I/R/RI Electrical Characteristics

(Refer to the test circuits,  $T_{MIN} \le T_J \le +125$ °C,  $I_O = 350$ mA,  $V_I = 33$ V, unless otherwise specified,  $C_I = 0.33$ mF,  $C_O = 0.1$ mF)

Parameter	Symbol	Conditions		Min.	Тур.	Max.	Units
Output Voltage	Vo	TJ=+25°C I <sub>O</sub> = 5 to 350mA V <sub>I</sub> = 27 to 38V		23	24	25	V
				22.8	24	25.2	
Line Regulation	ΔVο	Io = 200mA	V <sub>I</sub> = 27 to 38V	-	-	100	mV
		TJ =+25°C	VI = 28 to 38V	-	-	50	
Load Regulation	ΔVO	IO = 5mA to	0.5A, TJ =+25°C	-	-	480	mV
		IO = 5mA to	200mA, TJ =+25°C	-	-	240	
Quiescent Current	IQ	T <sub>J</sub> =+25°C		-	4.2	6	mA
Quiescent Current Change	ΔlQ	I <sub>O</sub> = 5mA to 350mA I <sub>O</sub> = 200mA V <sub>I</sub> = 27 to 38V		-	-	0.5	mA
				-	-	0.8	
Output Voltage Drift	ΔV/ΔΤ	I <sub>O</sub> = 5mA T <sub>J</sub> = 0 to +125°C		-	- 1.2	-	mV/°C
Output Noise Voltage	VN	f = 10Hz to 1	100KHz	-	170	-	mV/VO
Ripple Rejection	RR	f = 120Hz, IO = 300mA VI = 28 to 38V		50	-	-	dB
Dropout Voltage	VD	TJ =+25°C, IO = 500mA		-	2	-	V
Short Circuit Current	Isc	T <sub>J</sub> = +25 °C,	V <sub>I</sub> = 35V	-	300	-	mA
Peak Current	IPK	TJ =+25°C		-	700	-	mA

### NOTE:

1. TMIN:

KA78MXX/RI:  $T_{MIN} = -40$ °C KA78MXX/R:  $T_{MIN} = 0$ °C

# **Typical Applications**

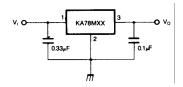


Figure 1. Fixed Output Regulator

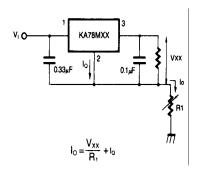


Figure 2. Constant Current Regulator

### Notes:

- 1. To specify an output voltage, substitute voltage value for "XX"
- 2. Although no output capacitor is needed for stability, it does improve transient response.
- 3. Required if regulator is located an appreciable distance from power Supply filter

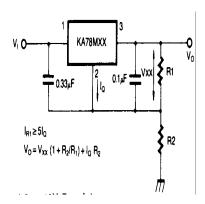


Figure 3. Circuit for Increasing Output Voltage

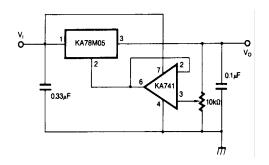


Figure 4. Adjustable Output Regulator (7 to 30V)

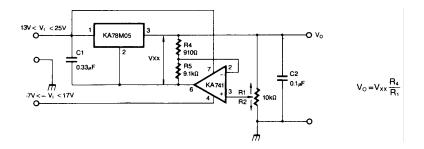
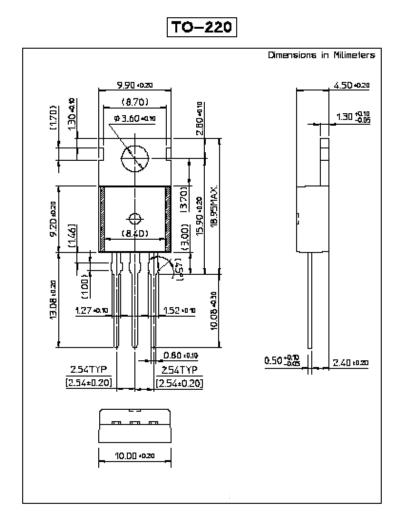


Figure 5. 0.5 to 10V Regulator

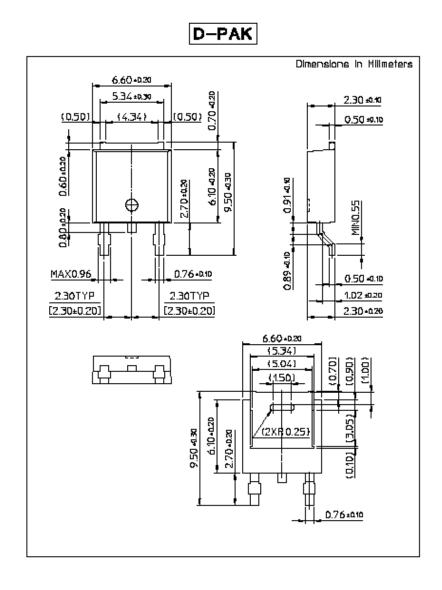
# **Ordering Information**

Device	Package	Operating Temperature
MC78MXXCT (LM78XXCT) (KA78MXX)	TO-220	0 ~ + 125°C
KA78MXXI		-40 ~ +125°C
MC78MXXCDT (KA78MXXR)	D-PAK	0 ~ + 125°C
KA78MXXRI		-40 ~ + 125°C

# **Package Dimensions**



# Package Dimensions (Continued)



# LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com

# 3-TERMINAL 0.5A POSITIVE VOLTAGE REGULATORS

The LM78MXXC/I series of three-terminal positive regulators are available in the TO-220 package with several fixed output voltages making it useful in a wide range of applications.

# 1:Input 2: GND 3: Output

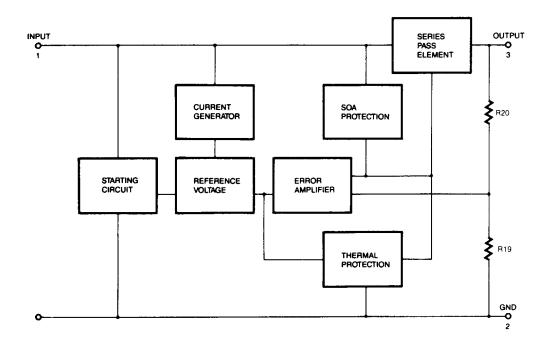
# **FEATURES**

- Output Current up to 0.5A
- Output Voltages of 5; 6; 8; 10; 12; 15; 18; 20; 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor SOA Protection
- Industrial and commercial temperature range

# **ORDERING INFORMATION**

Device	Package	Operating Temperature
LM78MXXT	TO-220	0 ~ + 125°C
LM78MXXIT	TO-220	- 40 ~ +125°C

# **BLOCK DIAGRAM**





Rev. B

©1999 Fairchild Semiconductor Corporation

Characteristic	Symbol	Value	Unit
Input Voltage (for V <sub>O</sub> = 5V to 18V)	VI	35	V
(for $V_0 = 24V$ )	$V_{I}$	40	V
Thermal Resistance Junction-Cases	R <sub>EJC</sub>	5	°C /W
Thermal Resistance Junction-Air	R <sub>EJA</sub>	65	°C /W
Operating Temperature Range KA78XXI	<b>-</b>	-40~ + 125	°C
KA78XX	T <sub>OPR</sub>	0~ + 125	°C
Storage Temperature Range	T <sub>STG</sub>	-65~ + 150	°C

# LM78M05/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits,  $T_{MIN}$   $T_{J}$  125°C,  $I_{O}$ =350mA,  $V_{I}$ =10V, unless otherwise specified,  $C_{I}$  = 0.33 $\mu$ F,  $C_{O}$ =0.1 $\mu$ F)

Characteristic	Symbol	Test Conditions		Min	Тур	Max	Unit
		T <sub>J</sub> = 25°C		4.8	5	5.2	
Output Voltage	Vo	$I_0 = 5 \text{ to } 350\text{mA}$ $V_1 = 7 \text{ to } 20\text{V}$		4.75	5	5.25	V
Line Regulation	$\Delta V_{O}$	I <sub>O</sub> = 200mA	V <sub>I</sub> = 7 to 25V			100	mV
Line Regulation	o	T <sub>J</sub> = 25°C	$V_1 = 8 \text{ to } 25V$			50	IIIV
Load Regulation	$\Delta V_{O}$	$I_0 = 5 \text{mA to } 0.5$	A, T <sub>J</sub> = 25°C			100	mV
Load Regulation	Δν <sub>0</sub>	I <sub>O</sub> = 5mA to 200mA, T <sub>J</sub> = 25°C				50	IIIV
Quiescent Current	lα	T <sub>J</sub> = 25°C			4.0	6	mA
		$I_O = 5mA$ to $350mA$				0.5	
Quiescent Current Change	$\Delta l_Q$	$I_0 = 200 \text{mA}$ $V_1 = 8 \text{ to } 25 \text{V}$				0.8	mA
Output Voltage Drift	$\frac{\Delta V_{O}}{\Delta T}$	$I_0 = 5mA$ $T_J = 0 \text{ to } 125^{\circ}C$			- 0.5		mV/°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to 100	KHz		40		μV
Ripple Rejection	RR	f = 120Hz, I <sub>O</sub> = 300mA V <sub>I</sub> = 8 to 18V		62			dB
Dropout Voltage	$V_D$	$T_J = 25^{\circ}C, I_O = 500mA$			2		V
Short Circuit Current	I <sub>SC</sub>	$T_J = 25^{\circ}C, V_I = 3$	55V		300		mA
Peak Current	$I_{PK}$	T <sub>J</sub> = 25°C	•		700		mA

<sup>\*</sup> T<sub>MIN</sub> T<sub>J</sub> T<sub>MAX</sub> LM78MXXI:T<sub>MIN</sub>=-40°C, T<sub>MAX</sub> = +125°C



LM78MXX: T<sub>MIN</sub>=0°C, T<sub>MAX</sub> = +125°C

\* Load and line regulation are specified at constant junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# LM78M06/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits,  $T_{MIN}$   $T_{J}$  125°C,  $I_{O}$ =350mA,  $V_{I}$ =11V, unless otherwise specified,  $C_{I}$  = 0.33 $\mu$ F,  $C_{O}$ =0.1 $\mu$ F)

Characteristic	Symbol	Test (	Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> = 25°C	T <sub>.J</sub> = 25°C		6	6.25	
Output Voltage	Vo	I <sub>O</sub> = 5 to 350mA V <sub>I</sub> = 8 to 21V		5.7	6	6.3	V
Line Regulation	$\Delta V_{O}$	I <sub>O</sub> = 200mA	$V_{I} = 8 \text{ to } 25V$			100	mV
	200	T <sub>J</sub> = 25°C	$V_1 = 9 \text{ to } 25V$			50	IIIV
Load Regulation	$\Delta V_{O}$	$I_0 = 5 \text{mA to } 0.5$	A, T <sub>J</sub> = 25°C			120	mV
Load Rogaldiion	70	$I_O = 5$ mA to 200mA, $T_J = 25$ °C				60	111.0
Quiescent Current	lα	T <sub>J</sub> = 25°C			4.0	6	mA
		$I_O = 5$ mA to $350$ mA				0.5	
Quiescent Current Change	$\Delta I_Q$	$I_0 = 200 \text{mA}$ $V_1 = 9 \text{ to } 25 \text{V}$				0.8	mA
Output Voltage Drift	$\frac{\Delta V_{O}}{\Delta T}$	$I_0 = 5mA$ $T_J = 0 \text{ to } 125^{\circ}C$	;		- 0.5		mV/°C
Output Noise Voltage	$V_N$	f = 10Hz to 100	KHz		45		μV
Ripple Rejection	RR	$f = 120Hz, I_0 = 300mA$ V <sub>1</sub> = 9 to 19V		59			dB
Dropout Voltage	$V_D$	$T_J = 25^{\circ}C, I_O =$	500mA		2		V
Short Circuit Current	I <sub>sc</sub>	$T_J = 25^{\circ}C, V_I = 3$	85V		300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> = 25°C			700		mA



<sup>\*</sup>T<sub>MIN</sub>
LM78MXXI:T<sub>MIN</sub>=-40°C
LM78MXX:T<sub>MIN</sub>=0°C
\* Load and line regulation are specified at constant, junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# LM78M08/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits,  $T_{MIN}$   $T_{J}$  125°C,  $I_{O}$ =350mA,  $V_{I}$ =14V, unless otherwise specified,  $C_{I}$  = 0.33 $\mu$ F,  $C_{O}$ =0.1 $\mu$ F)

Characteristic	Symbol	Test (	Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> = 25°C		7.7	8	8.3	
Output Voltage	Vo	$I_0 = 5 \text{ to } 350\text{m/s}$ $V_1 = 10.5 \text{ to } 23\text{V}$		7.6	8	8.4	V
Line Regulation	ΔVo	I <sub>O</sub> = 200mA	V <sub>I</sub> = 10.5 to 25V			100	mV
Line Regulation	Δν0	T <sub>J</sub> = 25°C	V <sub>I</sub> = 11 to 25V			50	IIIV
Load Degulation	41/	$I_0 = 5 \text{mA to } 0.5$	5A, T <sub>J</sub> = 25°C			160	ma\/
Load Regulation	$\Delta V_{O}$	I <sub>O</sub> = 5mA to 200mA, T <sub>J</sub> = 25°C				80	mV
Quiescent Current	ΙQ	T <sub>J</sub> = 25°C			4.0	6	mA
		$I_0 = 5mA$ to $350mA$				0.5	
Quiescent Current Change	$\Delta I_Q$	$I_O = 200 \text{mA}$ $V_I = 10.5 \text{ to } 25 \text{V}$				0.8	mA
Output Voltage Drift	$\frac{\Delta V_{O}}{\Delta T}$	$I_0 = 5mA$ $T_J = 0 \text{ to } 125^{\circ}C$			- 0.5		mV/°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to 100	)KHz		52		μV
Ripple Rejection	RR	f = 120Hz, I <sub>O</sub> = 300mA V <sub>I</sub> = 9 to 19V		56			dB
Dropout Voltage	$V_D$	$T_J = 25^{\circ}C, I_O =$	$T_J = 25^{\circ}C, I_O = 500 \text{mA}$		2		V
Short Circuit Current	I <sub>sc</sub>	T <sub>J</sub> = 25°C, V <sub>I</sub> = 3	35V		300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> = 25°C			700		mA

\*T<sub>MIN</sub>
LM78MXXI:T<sub>MIN</sub>=-40°C



LM78MXX:T<sub>MIN</sub>=0°C

\* Load and line regulation are specified at constant, junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# LM78M10/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits,  $T_{MIN}$   $T_{J}$  125°C,  $I_{O}$ =350mA,  $V_{I}$ =17V, unless otherwise specified,  $C_{I}$  = 0.33 $\mu$ F,  $C_{O}$ =0.1 $\mu$ F)

Characteristic	Symbol	Test Conditions		Min	Тур	Max	Unit
		T <sub>J</sub> = 25°C		9.6	10	10.4	
Output Voltage	Vo	I <sub>O</sub> = 5 to 350mA V <sub>I</sub> = 12.5 to 25V		9.5	10	10.5	V
Line Regulation	ΔVο	I <sub>O</sub> = 200mA	$V_{I}$ = 12.5 to 25V			100	mV
Line regulation	400	T <sub>J</sub> = 25°C	$V_1 = 13 \text{ to } 25V$			50	IIIV
Load Regulation	$\Delta V_{O}$	$I_0 = 5 \text{mA to } 0.5$	A, T <sub>J</sub> = 25°C			200	ma\/
Load Regulation	Δν0	$I_O = 5mA$ to 200mA, $T_J = 25^{\circ}C$				100	mV
Quiescent Current	ΙQ	T <sub>J</sub> = 25°C			4.1	6	mA
		$I_O = 5mA$ to $350mA$				0.5	
Quiescent Current Change	$\Delta I_Q$	I <sub>O</sub> = 200mA				0.8	mA
		V <sub>I</sub> = 12.5 to 25V				0.0	
Output Voltage Drift	$\Delta V_{O}$	$I_0 = 5mA$			- 0.5		mV/°C
	ΔΤ	$T_{\rm J} = 0 \text{ to } 125^{\circ}\text{C}$					, 0
Output Noise Voltage	$V_N$	f = 10Hz to 100	KHz		65		μV
Ripple Rejection	RR	f = 120Hz, I <sub>O</sub> =	300mA	55			dB
· inpplie i toje such		$V_1 = 13 \text{ to } 23V$			00		uВ
Dropout Voltage	$V_D$	$T_J = 25^{\circ}C, I_O = 500mA$			2		V
Short Circuit Current	I <sub>sc</sub>	T <sub>J</sub> = 25°C, V <sub>I</sub> = 3	85V		300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> = 25°C			700		mA



<sup>\*</sup>T<sub>MIN</sub>

LM78MXXI:T<sub>MIN</sub>=-40°C

LM78MXXT:T<sub>MIN</sub>=0°C

\* Load and line regulation are specified at constant, junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# LM78M12/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits,  $T_{MIN}$   $T_{J}$  125°C,  $I_{O}$ =350mA,  $V_{I}$ =19V, unless otherwise specified,  $C_{I}$  = 0.33 $\mu$ F,  $C_{O}$ =0.1 $\mu$ F)

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> = 25°C	11.5	12	12.5	
Output Voltage	Vo	I <sub>O</sub> = 5 to 350mA V <sub>I</sub> = 14.5 to 27V	11.5	12	12.6	V
Lines Regulation	$\Delta V_{O}$	I <sub>O</sub> = 200mA V <sub>I</sub> = 14.5 to 30V			100	mV
	2.0	$T_J = 25^{\circ}C$ $V_I = 16 \text{ to } 30V$			50	111 V
Load Regulation	$\Delta V_{O}$	$I_{O} = 5 \text{mA to } 0.5 \text{A}, T_{J} = 25^{\circ} \text{C}$			240	mV
Load Regulation		I <sub>O</sub> = 5mA to 200mA, T <sub>J</sub> = 25°C			120	1110
Quiescent Current	lα	T <sub>J</sub> = 25°C		4.1	6	mA
	$\Delta l_Q$	I <sub>O</sub> = 5mA to 350mA			0.5	
Quiescent Current Change		I <sub>O</sub> = 200mA			0.8	mA
		V <sub>I</sub> = 14.5 to 30V			0.6	
Output Voltage Drift	$\Delta V_{O}$	$I_O = 5mA$		- 0.5		mV/°C
Output Voltage Dilit	ΔΤ	$T_J = 0$ to $125^{\circ}C$		- 0.5		IIIV/ C
Output Noise Voltage	$V_N$	f = 10Hz to 100KHz		75		μV
Pipple Rejection	RR	f = 120Hz, I <sub>O</sub> = 300mA	55			٩D
Ripple Rejection	KK	$V_1 = 15 \text{ to } 25V$	55			dB
Dropout Voltage	V <sub>D</sub>	$T_J = 25^{\circ}C, I_O = 500mA$		2		<b>V</b>
Short Circuit Current	I <sub>sc</sub>	T <sub>J</sub> = 25°C, V <sub>I</sub> = 35V		300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> = 25°C		700		mA

<sup>\*</sup>T<sub>MIN</sub>

LM78MXXI:T<sub>MIN</sub>=-40°C



LM78MXX:T<sub>MIN</sub>=0°C

\* Load and line regulation are specified at constant, junction temperature. Change in V<sub>0</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# LM78M15/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits,  $T_{MIN}$   $T_{J}$  125°C,  $I_{O}$ =350mA,  $V_{I}$ =23V, unless otherwise specified,  $C_{I}$  = 0.33 $\mu$ F,  $C_{O}$ =0.1 $\mu$ F)

Characteristic	Symbol	Test	Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> = 25°C	T <sub>J</sub> = 25°C		15	15.6	
Output Voltage	Vo	$I_O = 5 \text{ to } 350 \text{m}.$ $V_I = 17.5 \text{ to } 30 \text{ N}.$		14.25	15	15.75	V
Line Regulation	ΔVo	I <sub>O</sub> = 200mA	$V_i$ = 17.5 to 30V			100	mV
Line Regulation		$T_J = 25^{\circ}C$	$V_1 = 20 \text{ to } 30V$			50	IIIV
Load Regulation	ΔVo	$I_0 = 5 \text{mA to } 0.5$	5A, T <sub>J</sub> = 25°C			300	mV
Load Regulation	2.0	$I_0 = 5 \text{mA to } 20$	0mA, T <sub>J</sub> = 25°C			150	] ""
Quiescent Current	lα	T <sub>J</sub> = 25°C			4.1	6	mA
	$\Delta I_Q$	I <sub>O</sub> = 5mA to 350mA				0.5	
Quiescent Current Change		I <sub>O</sub> = 200mA				0.8	mA
		V <sub>I</sub> = 17.5 to 30V				0.6	
Output Voltage Drift	$\Delta V_{O}$	$I_O = 5mA$			- 1		mV/°C
Output Voltage Drift	ΔΤ	$T_{\rm J} = 0 \text{ to } 125^{\circ}$			- !		IIIV/ C
Output Noise Voltage	$V_N$	f = 10Hz to 100	)KHz		100		μV
Ripple Rejection	RR	f = 120Hz, I <sub>O</sub> =	300mA	54			dB
Rippie Rejection	KK	$V_1 = 18.5 \text{ to } 28.5$	5V	54			
Dropout Voltage	$V_D$	$T_J = 25^{\circ}C, I_O = 500mA$			2		V
Short Circuit Current	I <sub>sc</sub>	$T_J = 25^{\circ}C, V_I = 1$	35V		300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> = 25°C			700		mA

\*T<sub>MIN</sub> LM78MXXI:T<sub>MIN</sub>=-40°C

LM78MXX:T<sub>MIN</sub>=0°C



<sup>\*</sup> Load and line regulation are specified at constant, junction temperature. Change in V<sub>0</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# LM78M18/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits,  $T_{MIN}$   $T_{J}$  125°C,  $I_{O}$ =350mA,  $V_{I}$ =26V, unless otherwise specified,  $C_{I}$  = 0.33 $\mu$ F,  $C_{O}$ =0.1 $\mu$ F)

Characteristic	Symbol	Test	Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> = 25°C	T <sub>J</sub> = 25°C		18	18.7	
Output Voltage	Vo	I <sub>O</sub> = 5 to 350mA V <sub>I</sub> = 20.5 to 33V		17.1	18	18.9	V
Line Regulation	$\Delta V_{O}$	$I_0 = 200 mA$	V <sub>I</sub> = 21 to 33V			100	mV
Line Regulation	Δ.0	T <sub>J</sub> = 25°C	$V_1 = 24 \text{ to } 33V$			50	IIIV
Load Regulation	ΔVo	$I_0 = 5 \text{mA to } 0.5$	5A, T <sub>J</sub> = 25°C			360	mV
Load Regulation	Δνο	$I_O = 5$ mA to 200mA, $T_J = 25$ °C				180	IIIV
Quiescent Current	ΙQ	T <sub>J</sub> = 25°C			4.2	6	mA
		I <sub>O</sub> = 5mA to 350mA				0.5	
Quiescent Current Change	$\Delta I_Q$	I <sub>O</sub> = 200mA				0.8	mA
		$V_1 = 21 \text{ to } 33V$	V <sub>I</sub> = 21 to 33V			0.6	
Output Voltage Drift	$\Delta V_{O}$	$I_0 = 5mA$			- 1.1		mV/°C
Output Voltage Dilit	ΔΤ	$T_J = 0$ to $125^{\circ}$ C			1.1		IIIV/°C
Output Noise Voltage	$V_N$	f = 10Hz to 100	OKHz		100		μV
Ripple Rejection	RR	f = 120Hz, I <sub>O</sub> =	300mA	53			dB
Ripple Rejection	KK	$V_1 = 22 \text{ to } 32V$		55			uБ
Dropout Voltage	$V_D$	$T_J = 25^{\circ}C, I_O = 500mA$			2		V
Short Circuit Current	I <sub>sc</sub>	T <sub>J</sub> = 25°C, V <sub>I</sub> =	35V		300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> = 25°C			700		mA



<sup>\*\*</sup>TMIN LM78MXXI:T<sub>MIN</sub>=-40°C
LM78MXX:T<sub>MIN</sub>=0°C
\*\*Load and line regulation are specified at constant, junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# LM78M20/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits, T<sub>MIN</sub> T<sub>J</sub> 125°C, I<sub>O</sub>=350mA, V<sub>I</sub>=29V, unless otherwise specified, C<sub>I</sub> = 0.33 $\mu$ F, C<sub>O</sub>=0.1 $\mu$ F)

Characteristic	Symbol	Test Conditions		Min	Тур	Max	Unit
		T <sub>J</sub> = 25°C		19.2	20	20.8	
Output Voltage	Vo	$I_0 = 5 \text{ to } 350 \text{m}$ $V_1 = 23 \text{ to } 35 \text{V}$	A	19	20	21	V
Line Regulation	$\Delta V_{O}$	I <sub>O</sub> = 200mA	V <sub>I</sub> = 23 to 35V			100	mV
Line Regulation	4.0	T <sub>J</sub> = 25°C	V <sub>I</sub> = 24 to 35V			50	IIIV
Load Regulation	$\Delta V_{O}$	$I_0 = 5mA \text{ to } 0.$	5A, T <sub>J</sub> = 25°C			400	mV
Load Regulation	Δνο	$I_0 = 5 \text{mA to } 20$	00mA, T <sub>J</sub> = 25°C			200	1117
Quiescent Current	ΙQ	T <sub>J</sub> = 25°C			4.2	6	mA
		I <sub>O</sub> = 5mA to 350mA				0.5	
Quiescent Current Change	$\Delta I_Q$	$I_0 = 200 \text{mA}$ $V_1 = 23 \text{ to } 35 \text{V}$				0.8	mA
Output Voltage Drift	$\frac{\Delta V_{O}}{\Delta T}$	I <sub>O</sub> = 5mA T <sub>J</sub> = 0 to 125°C			- 1.1		mV/°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to 10	0KHz		110		μV
Ripple Rejection	RR	f = 120Hz, I <sub>O</sub> = 300mA V <sub>I</sub> = 24 to 34V		53			dB
Dropout Voltage	V <sub>D</sub>	$T_J = 25^{\circ}C, I_O = 500mA$			2		V
Short Circuit Current	I <sub>SC</sub>	T <sub>J</sub> = 25°C, V <sub>I</sub> =	35V		300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> = 25°C			700		mA

\*T<sub>MIN</sub> LM78MXXI:T<sub>MIN</sub>=-40°C

LM78MXX:T<sub>MIN</sub>=0°C



<sup>\*</sup> Load and line regulation are specified at constant, junction temperature. Change in V<sub>0</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# LM78M24/I ELECTRICAL CHARACTERISTICS

(Refer to the test circuits,  $T_{MIN}$   $T_{J}$  125°C,  $I_{O}$ =350mA,  $V_{I}$ =33V, unless otherwise specified,  $C_{I}$  = 0.33 $\mu$ F,  $C_{O}$ =0.1 $\mu$ F)

Characteristic	Symbol	Test Conditions		Min	Тур	Max	Unit
		T <sub>J</sub> = 25°C		23	24	25	
Output Voltage	Vo	I <sub>O</sub> = 5 to 350mA V <sub>I</sub> = 27 to 38V		22.8	24	25.2	V
Line Regulation	$\Delta V_{O}$	I <sub>O</sub> = 200mA	V <sub>i</sub> = 27 to 38V			100	mV
Line Regulation	2.0	T <sub>J</sub> = 25°C	$V_1 = 28 \text{ to } 38V$			50	111.
Load Regulation	$\Delta V_{O}$	$I_0 = 5 \text{mA to } 0.5$	5A, T <sub>J</sub> = 25°C			480	mV
Load Regulation	200	I <sub>O</sub> = 5mA to 200mA, T <sub>J</sub> = 25°C				240	IIIV
Quiescent Current	lα	T <sub>J</sub> = 25°C			4.2	6	mA
		I <sub>O</sub> = 5mA to 350mA				0.5	
Quiescent Current Change	$\Delta I_{Q}$	I <sub>O</sub> = 200mA				0.8	mA
		V <sub>I</sub> = 27 to 38V					
Output Voltage Drift	$\Delta V_{O}$	$I_O = 5mA$			- 1.2		mV/°C
Odiput Voltage Dilit	ΔΤ	$T_J = 0 \text{ to } 125^{\circ}\text{C}$			- 1.2		IIIV/ C
Output Noise Voltage	$V_N$	f = 10Hz to 10	0KHz		170		μV
Ripple Rejection	RR	f = 120Hz, I <sub>O</sub> =	: 300mA	50			dB
Rippie Rejection	KK	$V_1 = 28 \text{ to } 38V$	50		30		uБ
Dropout Voltage	$V_D$	$T_J = 25^{\circ}C$ , $I_O = 500mA$			2		V
Short Circuit Current	I <sub>sc</sub>	T <sub>J</sub> = 25°C, V <sub>I</sub> =	35V		300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> = 25°C			700		mA

\*T<sub>MIN</sub>
LM78MXXI:T<sub>MIN</sub>=-40°C

LM78MXX:T<sub>MIN</sub>=0°C

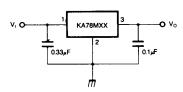


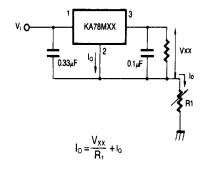
<sup>\*</sup> Load and line regulation are specified at constant, junction temperature. Change in V<sub>0</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# **APPLICATION CIRCUIT**

Fig. 1 Fixed output regulator

Fig. 2 Constant current regulator



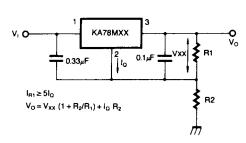


Notes:

- (1) To specify an output voltage, substitute voltage value for "XX".
- (2) Although no output capacitor is needed for stability, it does improve transient response.
- (3) Required if regulator is located an appreciable distance from power Supply filter.

Fig. 4 Adjustable output regulator (7 to 30V)

Fig. 3 Circuit for Increasing output voltage



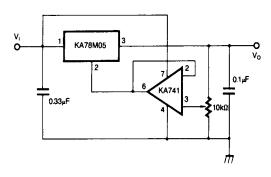
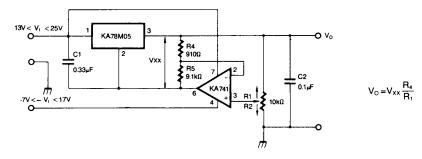


Fig. 5 0.5 to 10V Regulator





# **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

# **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

# LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

# **PRODUCT STATUS DEFINITIONS**

# **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

# **3-TERMINAL 1A NEGATIVE VOLTAGE REGULATORS**

The LM79XX series of three-terminal negative regulators are available in TO-220 package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible.

# TO-220 1: GND 2: Input 3: Output

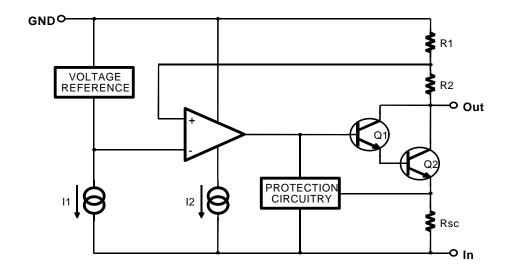
# **FEATURES**

- Output Current in Excess of 1A
- Output Voltages of -5, -6, -8, -12, -15, -18, -24V
- Internal Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe-Area Compensation

# **ORDERING INFORMATION**

Device	Output Voltage Tolerance	Package	Operating Temperature
LM79XXCT	± 4%	TO-220	0 405.00
LM79XXAT	± 2%	10 220	0 ~ +125°C

# **BLOCK DIAGRAM**





# ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=+25°C, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage	Vı	-35	V
Thermal Resistance Junction-Cases  Junction-Air	R <sub>θJC</sub> R <sub>θJA</sub>	5 65	°C /W
Operating Temperature Range	T <sub>OPR</sub>	0 ~ +125	°C
Storage Temperature Range	T <sub>STG</sub>	- 65 ~ +150	°C

# LM7905 ELECTRICAL CHARACTERISTICS

(V<sub>I</sub> = 10V, I<sub>O</sub> = 500mA,  $0^{\circ}$ C  $\leq$ T<sub>J</sub> $\leq$  +125 $^{\circ}$ C, C<sub>I</sub> =2.2 $\mu$ F, C<sub>O</sub> =1 $\mu$ F, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> =+25°C	- 4.8	- 5.0	- 5.2	
Output Voltage	Vo	$I_0 = 5mA \text{ to } 1A, P_0  15W$ $V_1 = -7 \text{ to } -20V$	- 4.75	-5.0	- 5.25	V
		$V_{I} = -7 \text{ to } -20V$ $I_{O} = 1A$		5	50	mV
Line Regulation	$\Delta V_{\Omega}$	$T_J = 25^{\circ}C$ $\frac{I_O = 1A}{V_I = -8 \text{ to -12V}}$ $I_O = 1A$		2	25	
Line Regulation		V <sub>I</sub> = -7.5 to -25V		7	50	
		$V_I$ = -8 to -12V $I_O$ =1A		7	50	
		I <sub>O</sub> = 5mA to 1.5A		10	100	
Load Regulation	$\Delta V_{O}$	$T_J = +25^{\circ}C$ $I_O = 250 \text{ to } 750\text{mA}$		3	50	mV
Quiescent Current	ΙQ	T <sub>J</sub> =+25°C		3	6	mA
Quiescent Current Change	$\Delta I_{O}$	I <sub>O</sub> = 5mA to 1A		0.05	0.5	mA
Quiescent ourient onlange	Q	$V_1 = -8 \text{ to } -25 \text{V}$		0.1	0.8	IIIA
Temperature Coefficient of V <sub>D</sub>	$\Delta V_{O}/\Delta T$	$I_O = 5mA$		- 0.4		mV/°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to $100KHzT_A = +25^{\circ}C$		40		μV
Ripple Rejection	RR	$f = 120Hz, I_0 = -35V$ $\Delta V_1 = 10V$	54	60		dB
Dropout Voltage	V <sub>D</sub>	$T_J=+25^{\circ}C$ $I_O=1A$		2		V
Short Circuit Current	I <sub>sc</sub>	$T_J = +25^{\circ}C, V_I = -35V$		300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+25°C		2.2		Α

<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Changes in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.



# **LM7906 ELECTRICAL CHARACTERISTICS**

 $(V_1 = 11V, I_0 = 500mA, 0^{\circ}C \le T_J \le +125^{\circ}C, C_1 = 2.2\mu F, C_0 = 1\mu F, unless otherwise specified.)$ 

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> = +25°C	- 5.75	- 6	- 6.25	
Output Voltage	Vo	$I_0 = 5mA \text{ to } 1A, P_0  15W$ $V_1 = -9 \text{ to } -21V$	- 5.7	- 6	- 6.3	V
Line Regulation	ΔVo	$T_J = 25^{\circ}C$ $V_i = -8 \text{ to } -25V$		10	120	mV
Line Regulation	Δνο	$V_{i}$ = - 9 to -12V		5	60	IIIV
		$T_J = + 25^{\circ}C$ $I_O = 5\text{mA to } 1.5\text{A}$		10	120	.,
Load Regulation	ΔV <sub>O</sub>	T <sub>J</sub> =+ 25°C I <sub>O</sub> = 250 to 750mA		3	60	mV
Quiescent Current	IQ	T <sub>J</sub> =+ 25°C		3	6	mA
Outposent Current Change	$\Delta I_Q$	I <sub>O</sub> = 5mA to 1A			0.5	A
Quiescent Current Change	ΔiQ	$V_1 = -9 \text{ to } -25 \text{V}$			1.3	mA
Temperature Coefficient of V <sub>D</sub>	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$		-0.5		mV/°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to $100$ KHz $T_A = + 25$ °C		130		μV
Ripple Rejection	RR	f = 120Hz $\Delta V_1 = 10V$	54	60		dB
Dropout Voltage	V <sub>D</sub>	T <sub>J</sub> =+ 25°C I <sub>O</sub> = 1A		2		V
Short Circuit Current	I <sub>SC</sub>	$T_J = +25^{\circ}C, V_I = -35V$		300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> = +25°C		2.2		Α

 $<sup>^*</sup>$  Load and line regulation are specified at constant junction temperature. Changes in  $V_O$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.



**LM7908 ELECTRICAL CHARACTERISTICS** (V<sub>I</sub> = 14V, I<sub>O</sub> = 500mA,  $0^{\circ}$ C  $\leq$ T<sub>J</sub> $\leq$  +125 $^{\circ}$ C, C<sub>I</sub> =2.2 $\mu$ F, C<sub>O</sub> = 1 $\mu$ F, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> =+ 25°C	- 7.7	- 8	- 8.3	
Output Voltage	Vo	$I_O = 5mA \text{ to } 1A, P_O 15W$ $V_I = -1.5 \text{ to } -23V$	- 7.6	- 8	- 8.4	V
Line Regulation	ΔVo	$V_{I} = -10.5 \text{ to } -25 \text{ V}$		10	100	mV
Line Regulation	Δνο	$T_J = 25^{\circ}C$ $V_i = -10.5 \text{ to } -25V$ $V_i = -11 \text{ to } -17V$		5	80	IIIV
1. 15 1.		$T_J = + 25^{\circ}C$ $I_O = 5mA \text{ to } 1.5A$		12	160	.,
Load Regulation	ΔVo	T <sub>J</sub> =+ 25°C I <sub>O</sub> = 250 to 750mA		4	80	mV
Quiescent Current	Ιq	T <sub>J</sub> =+ 25°C		3	6	mA
Quiescent Current Change	$\Delta I_{Q}$	$I_0 = 5mA$ to 1A		0.05	0.5	mA
Quiescent Current Change	ΔiQ	$V_1 = -11.5 \text{ to } -25 \text{V}$		0.1	1	IIIA
Temperature Coefficient of V <sub>D</sub>	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$		-0.6		mV/°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to 100KHz T <sub>A</sub> =+ 25°C		175		μV
Ripple Rejection	RR	$f = 120Hz$ $\Delta V_{I} = 10V$	54	60		dB
Dropout Voltage	$V_D$	T <sub>J</sub> =+ 25°C I <sub>O</sub> = 1A		2		V
Short Circuit Current	I <sub>sc</sub>	T <sub>J</sub> =+ 25°C, V <sub>I</sub> = -35V		300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+ 25°C		2.2		Α

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant junction temperature. Changes in  $V_0$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.



# **LM7909 ELECTRICAL CHARACTERISTICS**

 $(V_1 = 14V, I_0 = 500 \text{mA}, 0^{\circ}\text{C} \le T_J \le + 125^{\circ}\text{C}, C_1 = 2.2 \mu\text{F}, C_0 = 1 \mu\text{F}, unless otherwise specified})$ 

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> =+ 25°C	- 8.7	- 9.0	- 9.3	
Output Voltage	Vo	$I_O = 5mA \text{ to } 1A, P_O 15W$ $V_I = -1.5 \text{ to } -23V$	- 8.6	- 9.0	- 9.4	V
Line Regulation	$\Delta V_{O}$	$T_J = 25^{\circ}C$ $\frac{V_I = -10.5 \text{ to } -25V}{V_I = -11 \text{ to } -17V}$		10	180	mV
Line Regulation	70	$V_1 = 23 \text{ C}$ $V_1 = -11 \text{ to } -17 \text{ V}$		5	90	IIIV
		$T_J = + 25^{\circ}C$ $I_O = 5mA \text{ to } 1.5A$		12	180	
Load Regulation	ΔVo	T <sub>J</sub> =+ 25°C I <sub>O</sub> = 250 to 750mA		4	90	mV
Quiescent Current	lα	T <sub>J</sub> =+ 25°C		3	6	mA
Quiescent Current Change	$\Delta I_Q$	I <sub>O</sub> = 5mA to 1A		0.05	0.5	mA
Quiescent Current Change	ΔiQ	V <sub>I</sub> = -11.5 to -25V		0.1	1	IIIA
Temperature Coefficient of V <sub>D</sub>	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$		-0.6		mV/°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to 100KHz T <sub>A</sub> =+ 25°C		175		μV
Ripple Rejection	RR	$f = 120Hz$ $\Delta V_{I} = 10V$	54	60		dB
Dropout Voltage	V <sub>D</sub>	T <sub>J</sub> =+ 25°C I <sub>O</sub> = 1A		2		V
Short Circuit Current	I <sub>SC</sub>	T <sub>J</sub> = +25°C, V <sub>I</sub> = -35V		300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+25°C		2.2		Α

 $<sup>^*</sup>$  Load and line regulation are specified at constant junction temperature. Changes in  $V_0$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.



# **LM7912 ELECTRICAL CHARACTERISTICS**

(V<sub>I</sub>= 18V, I<sub>O</sub> =500mA,  $0^{\circ}$ C  $\leq$ T<sub>J</sub> $\leq$  +125 $^{\circ}$ C, C<sub>I</sub> =2.2 $\mu$ F, C<sub>O</sub> = 1 $\mu$ F, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
		$T_J = +25^{\circ}C$	-11.5	-12	-12.5	
Output Voltage	Vo	$I_O = 5mA \text{ to } 1A, P_O 15W$ $V_I = -15.5 \text{ to } -27V$	-11.4	-12	-12.6	V
Line Regulation	$\Delta V_{O}$	$T_J = 25^{\circ}C$ $V_I = -14.5 \text{ to } -30V$ $V_I = -16 \text{ to } -22V$		12	240	mV
Line Regulation	Δνο	$V_{i}$ = -16 to -22V		6	120	IIIV
		$T_J = + 25^{\circ}C$ $I_O = 5mA \text{ to } 1.5A$		12	240	.,
Load Regulation	ΔV <sub>O</sub>	$T_J = + 25^{\circ}C$ $I_O = 250 \text{ to } 750\text{mA}$		4	120	mV
Quiescent Current	ΙQ	T <sub>J</sub> =+ 25°C		3	6	mA
Outles sent Current Change	$\Delta I_{O}$	$I_O = 5$ mA to 1A		0.05	0.5	mA
Quiescent Current Change	ΔIQ	$V_{I} = -15 \text{ to } -30 \text{V}$		0.1	1	IIIA
Temperature Coefficient of V <sub>D</sub>	$\Delta V_{O}/\Delta T$	$I_O = 5mA$		-0.8		mV/°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to 100KHz T <sub>A</sub> =+ 25°C		200		μV
Ripple Rejection	RR	$f = 120Hz$ $\Delta V_I = 10V$	54	60		dB
Dropout Voltage	V <sub>D</sub>	$T_J = +25^{\circ}C$ $I_O = 1A$		2		V
Short Circuit Current	I <sub>SC</sub>	$T_J = + 25^{\circ}C, V_I = -35V$		300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+ 25°C		2.2		Α

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant junction temperature. Changes in  $V_0$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.



# **LM7915 ELECTRICAL CHARACTERISTICS**

 $(V_1 = 23V, I_0 = 500mA, 0^{\circ}C \le T_J + 125^{\circ}C, C_1 = 2.2\mu F, C_0 = 1\mu F, unless otherwise specified.)$ 

Characteristic	Symbol	Tes	st Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> =+ 25°C	T <sub>J</sub> =+ 25°C		-15	-15.6	
Output Voltage	Vo	$I_0 = 5 \text{mA to}$ $V_1 = -18 \text{ to } -$	1A, P <sub>O</sub> 15W 30V	-14.25	-15	-15.75	V
Line Regulation	$\Delta V_{\Omega}$	T <sub>J</sub> = 25°C	$V_1 = -17.5 \text{ to } -30 \text{V}$		12	300	mV
Ellie Regulation	Δν0	1,5 – 20 0	$V_{i}$ = -20 to -26V		6	150	IIIV
Load Decidation		$T_J = + 25$ °C $I_O = 5$ mA to	1.5A		12	300	\/
Load Regulation	ΔV <sub>O</sub>	$T_J = + 25^{\circ}C$ $I_O = 250 \text{ to } T$			4	150	mV
Quiescent Current	ΙQ	T <sub>J</sub> =+ 25°C			3	6	mA
Quiescent Current Change	Al	$I_0 = 5 \text{mA to}$	1A		0.05	0.5	mA
Quiescent Current Change	$\Delta I_Q$	$V_1 = -18.5 \text{ to}$	o -30V		0.1	1	1117 (
Temperature Coefficient of V <sub>D</sub>	$\Delta V_{O}/\Delta T$	$I_O = 5mA$			-0.9		mV/°C
Output Noise Voltage	V <sub>N</sub>	$f = 10Hz$ to $T_A = + 25$ °C			250		μV
Ripple Rejection	RR	f = 120Hz $\Delta V_I = 10V$		54	60		dB
Dropout Voltage	V <sub>D</sub>	$T_J=+25^{\circ}C$ $I_O=1A$			2		V
Short Circuit Current	I <sub>SC</sub>	T <sub>J</sub> =+ 25°C,	V <sub>I</sub> = -35V		300		mA
Peak Current	$I_{PK}$	T <sub>J</sub> =+ 25°C			2.2		Α

<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Changes in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.



# **LM7918 ELECTRICAL CHARACTERISTICS**

(V<sub>I</sub> = 27V, I<sub>O</sub> = 500mA,  $0^{\circ}$ C  $\leq$ T<sub>J</sub> $\leq$ +125 $^{\circ}$ C, C<sub>I</sub> =2.2 $\mu$ F, C<sub>O</sub> = 1 $\mu$ F, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> =+ 25°C	-17.3	-18	-18.7	
Output Voltage	Vo	$I_O = 5mA \text{ to } 1A, P_O 15W$ $V_I = -22.5 \text{ to } -33V$	-17.1	-18	-18.9	V
Line Regulation	$\Delta V_{O}$	$T_{ij} = 25^{\circ}C$ $V_{ij} = -21 \text{ to } -33V$		15	360	mV
Line regulation	400	$V_{i}$ = -24 to -30V		8	180	IIIV
15 15		$T_J = + 25^{\circ}C$ $I_O = 5mA \text{ to } 1.5A$		15	360	
Load Regulation	ΔVo	T <sub>J</sub> =+ 25°C I <sub>O</sub> = 250 to 750mA		5	180	mV
Quiescent Current	lα	T <sub>J</sub> =+ 25°C		3	6	mA
0	4.1	$I_O = 5mA$ to 1A			0.5	mA
Quiescent Current Change	$\Delta I_{Q}$	$V_1 = -22 \text{ to } -33 \text{V}$			1	IIIA
Temperature Coefficient of V <sub>D</sub>	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$		-1		mV/°C
Output Noise Voltage	$V_N$	f = 10Hz to 100KHz T <sub>A</sub> =+ 25°C		300		μV
Ripple Rejection	RR	$f = 120Hz$ $\Delta V_1 = 10V$	54	60		dB
Dropout Voltage	V <sub>D</sub>	$T_J$ =+ 25°C $I_O$ = 1A		2		V
Short Circuit Current	Isc	T <sub>J</sub> =+ 25°C, V <sub>I</sub> = -35V		300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+ 25°C		2.2		Α

<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Changes in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.



# **LM7924 ELECTRICAL CHARACTERISTICS**

(V<sub>I</sub> = 33V, I<sub>O</sub> = 500mA,  $0^{\circ}$ C  $\leq$ T<sub>J</sub> $\leq$ +125 $^{\circ}$ C, C<sub>I</sub> =2.2 $\mu$ F, C<sub>O</sub> = 1 $\mu$ F, unless otherwise specified.)

Characteristic	Symbol	Tes	st Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> =+25°C	T <sub>J</sub> =+25°C		- 23 - 24	- 25	
Output Voltage	Vo	-	$I_{O} = 5\text{mA to 1A}, P_{O} \le 15\text{W}$ V <sub>I</sub> = -27 to -38V		- 24	- 25.2	٧
Line Regulation	ΔVo	T <sub>J</sub> = 25°C	$V_1 = -27 \text{ to } -38 \text{V}$		15	480	mV
Line Regulation	200	1) = 25 C	$V_{I}$ = - 30 to - 36V		8	180	IIIV
Load Damidation		$T_J = +25^{\circ}C$ $I_O = 5mA$ to	1.5A		15	480	
Load Regulation	ΔV <sub>O</sub>	$T_J = + 25^{\circ}C$ $I_O = 250 \text{ to } T_{O}$			5	240	mV
Quiescent Current	lα	T <sub>J</sub> =+ 25°C			3	6	mA
Ouisseent Current Change	$\Delta I_Q$	$I_0 = 5mA$ to	1A			0.5	mA
Quiescent Current Change	ΔiQ	$V_1 = -27 \text{ to } -$	38V			1	ША
Temperature Coefficient of V <sub>D</sub>	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$			-1		mV/°C
Output Noise Voltage	$V_N$	f = 10Hz to $T_A = + 25$ °C			400		μV
Ripple Rejection	RR	f = 120Hz $\Delta V_1 = 10V$		54	60		dB
Dropout Voltage	V <sub>D</sub>	T <sub>J</sub> = +25°C I <sub>O</sub> = 1A			2		V
Short Circuit Current	I <sub>sc</sub>	T <sub>J</sub> =+ 25°C, V <sub>I</sub> = -35V			300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+25°C	•		2.2		Α

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant junction temperature. Changes in  $V_0$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.



# LM7905A ELECTRICAL CHARACTERISTICS

(V<sub>I</sub> = 10V, I<sub>O</sub> = 500mA,  $0^{\circ}$ C  $\leq$ T<sub>J</sub> $\leq$  +125 $^{\circ}$ C, C<sub>I</sub> =2.2 $\mu$ F, C<sub>O</sub> =1 $\mu$ F, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> =+ 25°C	- 4.9	- 5.0	- 5.1	
Output Voltage	Vo	$I_0 = 5mA \text{ to } 1A, P_0  15W$ $V_1 = -7 \text{ to } -20V$	- 4.8	-5.0	- 5.2	V
		$V_1 = -7 \text{ to } -20V$ $I_0 = 1A$		5	50	mV
Line Regulation	$\Delta V_{\Omega}$	$T_J = +25^{\circ}C$ $\frac{I_0=1A}{V_1 = -8 \text{ to } -12V}$ $I_0=1A$		2	25	
Line Regulation		V <sub>I</sub> = -7.5 to -25V		7	50	
		$V_i$ = -8 to -12V $I_O$ =1A		7	50	
		$I_O = 5$ mA to 1.5A		10	100	
Load Regulation	$\Delta V_{O}$	$T_J = +25^{\circ}C$ $I_O = 250 \text{ to } 750\text{mA}$		3	50	mV
Quiescent Current	ΙQ	T <sub>J</sub> = +25°C		3	6	mA
Quiescent Current Change	$\Delta I_{O}$	I <sub>O</sub> = 5mA to 1A		0.05	0.5	mA
Quiescent ounent onlange		$V_1 = -8 \text{ to } -25 \text{V}$		0.1	8.0	IIIA
Temperature Coefficient of V <sub>D</sub>	$\Delta V_{O}/\Delta T$	$I_O = 5mA$		- 0.4		mV/°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to $100KHzT_A = + 25°C$		40		μV
Ripple Rejection	RR	$f = 120Hz, I_0 = -35V$ $\Delta V_1 = 10V$	54	60		dB
Dropout Voltage	V <sub>D</sub>	$T_J = + 25^{\circ}C$ $I_O = 1A$		2		V
Short Circuit Current	I <sub>SC</sub>	T <sub>J</sub> =+ 25°C, V <sub>I</sub> = -35V		300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+ 25°C		2.2		Α

<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Changes in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.



(V<sub>I</sub>= 18V, I<sub>O</sub>=500mA,  $0^{\circ}$ C  $\leq$ T<sub>J</sub> $\leq$  +125 $^{\circ}$ C, C<sub>I</sub>=2.2 $\mu$ F, C<sub>O</sub> = 1 $\mu$ F, unless otherwise specified.)

Characteristic	Symbol	Test Conditions	Min	Тур	Max	Unit
		T <sub>J</sub> =+ 25°C	-11.75	-12	-12.25	
Output Voltage	Vo	$I_O = 5mA \text{ to } 1A, P_O 15W$ $V_I = -15.5 \text{ to } -27V$	-11.5	-12	-12.5	V
Line Regulation	$\Delta V_{O}$	$T_J = +25^{\circ}C$ $V_i = -14.5 \text{ to } -30V$		12	240	mV
Line Regulation	ΔVO	$V_{i}$ = -16 to -22V		6	120	IIIV
		$T_J = +25^{\circ}C$ $I_O = 5mA$ to 1.5A		12	240	,
Load Regulation	ΔV <sub>O</sub>	T <sub>J</sub> =+ 25°C I <sub>O</sub> = 250 to 750mA		4	120	mV
Quiescent Current	ΙQ	T <sub>J</sub> =+ 25°C		3	6	mA
Outcomet Current Change	$\Delta I_Q$	$I_0 = 5mA$ to 1A		0.05	0.5	mA
Quiescent Current Change		V <sub>I</sub> = -15 to -30V		0.1	1	IIIA
Temperature Coefficient of V <sub>D</sub>	$\Delta V_O/\Delta T$	$I_0 = 5mA$		-0.8		mV/°C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz to $100$ Khz $T_A = + 25$ °C		200		μV
Ripple Rejection	RR	f = 120Hz $\Delta V_1 = 10V$	54	60		dB
Dropout Voltage	V <sub>D</sub>	T <sub>J</sub> =+ 25°C I <sub>O</sub> = 1A		2		V
Short Circuit Current	I <sub>sc</sub>	T <sub>J</sub> =+ 25°C, V <sub>I</sub> = -35V		300		mA
Peak Current	$I_{PK}$	T <sub>J</sub> =+ 25°C		2.2		Α

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant junction temperature. Changes in  $V_0$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.

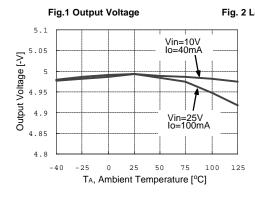


(V<sub>1</sub> = 23V, I<sub>O</sub> = 500mA,  $0^{\circ}$ C  $\leq$ T<sub>J</sub> $\leq$  +125 $^{\circ}$ C, C<sub>1</sub>=2.2 $\mu$ F, C<sub>O</sub> = 1 $\mu$ F, unless otherwise specified.)

Characteristic	Symbol	Test Conditions		Min	Тур	Max	Unit
		T <sub>J</sub> = +25°C		-14.7	-15	-15.3	
Output Voltage	Vo	I <sub>O</sub> = 5mA to 1A, P <sub>O</sub> 15W V <sub>I</sub> = -18 to -30V		-14.4	-15	-15.6	V
Line Regulation	ΔVo	T <sub>.1</sub> =+25°C	$V_1 = -17.5 \text{ to } -30 \text{V}$		12	300	mV
Line Regulation	200		/ <sub>I</sub> = -20 to -26V		6	150	IIIV
Load Decidation		$T_J = + 25^{\circ}C$ $I_O = 5mA \text{ to } 1.5$	$T_J = + 25^{\circ}C$ $I_O = 5mA \text{ to } 1.5A$		12	300	.,
Load Regulation	ΔVo	T <sub>J</sub> =+ 25°C I <sub>O</sub> = 250 to 750mA			4	150	mV
Quiescent Current	ΙQ	T <sub>J</sub> =+ 25°C			3	6	mA
Quiescent Current Change	41	I <sub>O</sub> = 5mA to 1A			0.05	0.5	mA
Quiescent Current Change	$\Delta I_Q$	$V_1 = -18.5 \text{ to } -3$	30V		0.1	1	ША
Temperature Coefficient of V <sub>D</sub>	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$			-0.9		mV/°C
Output Noise Voltage	$V_N$	f = 10Hz  to  10 $T_A = +25^{\circ}C$	0KHz		250		μV
Ripple Rejection	RR	f = 120Hz $\Delta V_I = 10$ V		54	60		dB
Dropout Voltage	V <sub>D</sub>	T <sub>J</sub> = +25°C I <sub>O</sub> = 1A			2		V
Short Circuit Current	I <sub>sc</sub>	T <sub>J</sub> =+ 25°C, V <sub>I</sub> = -35V			300		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> =+ 25°C	•		2.2		Α

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant junction temperature. Changes in  $V_{0}$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.





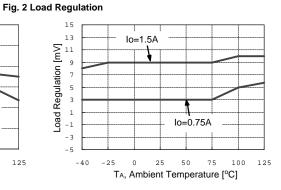
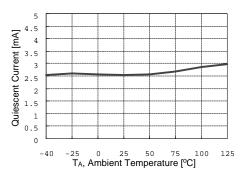


Fig.3 Quiescent Current

Fig. 4 Dropout Voltage



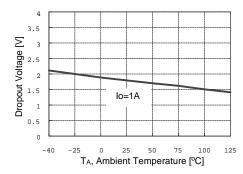


Fig.5 Short Circuit Current

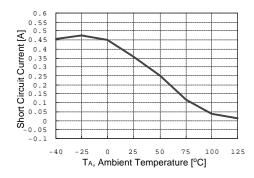
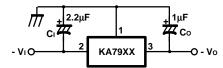




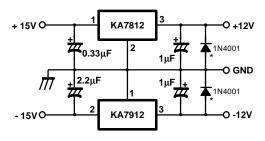
Fig. 6 Negative Fixed output regulator



# Notes:

- (1) To specify an output voltage, substitute voltage value for "XX "
- (2) Required for stability. For value given, capacitor must be solid tantalum. If aluminum electronics are used, at least ten times value shown should be selected. C<sub>I</sub> is required if regulator is located an appreciable
- distance from power supply filter.
- (3) To improve transient response. If large capacitors are used, a high current diode from input to output (1N400l or similar) should be introduced to protect the device from momentary input short circuit.

Fig. 7 Split power supply (±12V/1A)



<sup>\*:</sup> Against potential latch-up problems.



# **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

# **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

# LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

# **PRODUCT STATUS DEFINITIONS**

# **Definition of Terms**

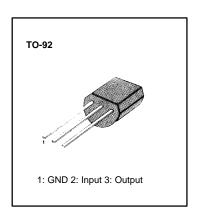
Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

# **3-TERMINAL 0.1A NEGATIVE VOLTAGE REGULATORS**

These regulators employ internal current limiting and thermal shutdown, making them essentially indestructible.

# **FEATURES**

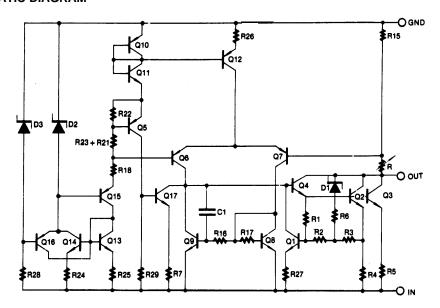
- Output current up to 100mA
- · No external components
- Internal thermal over load protection
- Internal short circuit current limiting
   Output Voltage Offered in ± 5% Tolerance
- Output Voltage of -5V,-12V,-15V,-18V and -24V



# **ORDERING INFORMATION**

Device	Package	Operating Temperature
MC79LXXACP (LM79LXXACZ) KA79LXXAZ	TO - 92	0 ~ + 125°C

# **SCHEMATIC DIAGRAM**





# **ABSOLUTE MAXIMUM RATINGS** ( $T_A = +25^{\circ}C$ , unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage (-5V)		-30	
(-12V to -18V)	$V_{I}$	-35	$V_{DC}$
(-24V)		-40	
Operating Temperature Range	T <sub>OPR</sub>	0 ~ +125	°C
Storage Temperature Range	T <sub>STG</sub>	-65 ~ +150	°C

# MC79L05A ELECTRICAL CHARACTERISTICS

 $(V_{I} = \text{-}10\text{V}, \, I_{O} = 40\text{mA}, \, C_{I} = 0.33 \mu\text{F}, \, C_{O} = 0.1 \mu\text{F}, \, 0^{\circ}\text{C} \leq T_{J} \leq \text{+}125^{\circ}\text{C}, \, \text{unless otherwise specified})$ 

Charact	eristic	Symbol	Test	Conditions	Min	Тур	Max	Unit
Output Voltage		Vo	T <sub>J</sub> = +25°C		- 4.8	- 5.0	- 5.2	V
I. B. I.				-7.0V ≥ V <sub>I</sub> ≥-20V		15	150	
I ine Regulation		$\Delta V_{O}$	T <sub>J</sub> =+25°C	-8V ≥ V <sub>I</sub> ≥-20V			100	mV
		ΔVο	T <sub>J</sub> =+25°C	$1.0\text{mA} \le I_0 \le 100\text{mA}$		20	60	.,
Load Regulation		Δνο	1J=+25°C	$1.0mA \le I_0 \le 40mA$		10	30	mV
Output Voltage	Output Voltage		-7.0V>V <sub>I</sub> >-20V, 1.0mA≤ I <sub>O</sub> ≤40mA		- 4.75		- 5.25	.,
Output voitage			$V_1 = -10V$ , $1.0mA \le I_0 \le 70mA$		- 4.75		- 5.25	V
0			$T_J = +25^{\circ}C$			2.0	6.0	mA
Quiescent Current		lα	T <sub>J</sub> = +125°C				5.5	IIIA
Quiescent	With Line	4.1	-8V≥ V <sub>I</sub> ≥-20V				1.5	
Current Change	With Load	$\Delta I_Q$	1.0mA≤ I <sub>O</sub> ≤40mA				0.1	mA
Output Noise Volta	age	V <sub>N</sub>	$T_A = +25^{\circ}C,10Hz \le f \le 100KHz$			30		μV
Ripple Rejection		RR	$f = 120Hz, -8V \ge V_1 \ge -18V$ $T_J = +25^{\circ}C$		41	60		dB
		IXIX			71	00		uБ
Dropout Voltage		V <sub>D</sub>	T <sub>J</sub> = +25°C			1.7		V

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.



# MC79L12A ELECTRICAL CHARACTERISTICS

 $(V_{\text{I}} = \text{-}19V, \ I_{\text{O}} = 40\text{mA}, \ C_{\text{I}} = 0.33 \mu\text{F}, \ C_{\text{O}} = 0.1 \mu\text{F}, \ 0^{\circ}\text{C} \leq T_{\text{J}} \leq +125^{\circ}\text{C}, \ unless \ otherwise \ specified)$ 

Characte	ristic	Symbol	Tes	t Conditions	Min	Тур	Max	Unit
Output Voltage		Vo	T <sub>J</sub> = +25°C		-11.5	-12.0	-12.5	V
			T.ı =+25°C	-14.5V ≥V <sub>I</sub> ≥-27V			250	
Line Regulation		$\Delta V_{O}$	1 J = +23 C	-16V≥V <sub>I</sub> ≥-27V			200	mV
		$\Delta V_{\Omega}$	T. =+25°C	1.0mA≤ l <sub>0</sub> ≤100mA			100	
Load Regulation	Load Regulation		1J =+25 C	1.0mA≤ I <sub>O</sub> ≤40mA			50	mV
Output Valtage			-14.5V>V <sub>I</sub> >-27V, 1.0mA≤I <sub>O</sub> ≤40mA		-11.4		-12.6	
Output Voltage		Vo	$V_1 = -19V, 1.0 \text{mA} \le I_0 \le 70 \text{mA}$		-11.4		-12.6	V
Quiescent Current		lα	T <sub>J</sub> = +25°C				6.5	
Quiescent Curren	l		T <sub>J</sub> = +125°C				6.0	mA
Quiescent	With Line	A.I.	-16V≥V <sub>I</sub> ≥-27V				1.5	
Current Change	With Load	$\Delta I_Q$	1.0mA≤ I <sub>O</sub> ≤40mA				0.1	mA
Output Noise Volt	age	V <sub>N</sub>	T <sub>A</sub> = +25°C,10Hz f 100KHz			80		μV
Ripple Rejection		RR	f = 120Hz, -150V≥ $V_1$ ≥-25V T <sub>J</sub> = +25°C		37	42		dB
		INN			37	42		aB
Dropout Voltage		$V_D$	$T_J = +25^{\circ}C$			1.7		V

<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# MC79L15A ELECTRICAL CHARACTERISTICS

 $(V_{I} = -23V, \ I_{O} = 40 mA, \ C_{I} = 0.33 \mu F, \ C_{O} = 0.1 \mu F, \ 0^{\circ}C \le T_{J} \le +125^{\circ}C, \ unless \ otherwise \ specified)$ 

Character	ristic	Symbol	Tes	t Conditions	Min	Тур	Max	Unit
Output Voltage		Vo	T <sub>J</sub> = +25°C		-14.4	-15.0	-15.6	V
		41/	T <sub>.1</sub> =+25°C	-17.5V≥V <sub>I</sub> ≥-30V			300	mV
Line Regulation		$\Delta V_{O}$	11 - 125 0	-27V≥V <sub>I</sub> ≥-30V			250	
		41/	T.ı =+25°C	1.0mA≤ I <sub>O</sub> ≤100mA			150	
Load Regulation		$\Delta V_{O}$	1) =+25 C	1.0mA≤ I <sub>O</sub> ≤40mA			75	mV
			-17.5V>V <sub>I</sub> >-30V, 1.0mA≤ I <sub>O</sub> ≤40mA		-14.25		-15.75	
Output Voltage		Vo	$V_1 = -23V$ , $1.0mA \le I_0 \le 70mA$		-14.25		-15.75	V
Quiescent Current		lα	$T_J = +25^{\circ}C$				6.5	A
Quiescent Current			T <sub>J</sub> = +125°C				6.0	mA
Quiescent	With Line	4.1	-20V≥V <sub>I</sub> ≥-30V				1.5	
Current Change	With Load	$\Delta I_Q$	1.0mA≤ I <sub>O</sub> ≤40mA				0.1	mA
Output Noise Volta	age	$V_N$	T <sub>A</sub> = 25°C,10Hz≤f≤100KHz			90		μV
Ripple Rejection		RR	f = 120Hz, -18.5V≥ V₁≥-28.5V		34	39		dB
		IXIX	T <sub>J</sub> = +25°C		34	39		ub
Dropout Voltage		$V_D$	$T_J = +25^{\circ}C$			1.7		V

<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Change in V<sub>0</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.



# MC79L18A ELECTRICAL CHARACTERISTICS

 $(V_{\text{I}} = \text{-27V}, \, I_{\text{O}} = 40 \text{mA}, \, C_{\text{I}} = 0.33 \mu F, \, C_{\text{O}} = 0.1 \mu F, \, 0^{\circ} C \leq T_{\text{J}} \leq +125^{\circ} C, \, \text{unless otherwise specified})$ 

Charact	teristic	Symbol	Test	Conditions	Min	Тур	Max	Unit
Output Voltage		Vo	T <sub>J</sub> =+25°C		-17.3	-18.0	-18.7	V
			T .25°C	-20.7V≥ V <sub>I</sub> ≥-33V			325 mV	
Line Regulation		$\Delta V_{O}$	T <sub>J</sub> =+25°C	-21V≥ V <sub>I</sub> ≥-33V			275	mv
			T <sub>.1</sub> =+25°C	1.0mA≤ I <sub>O</sub> ≤100mA			170	mV
Load Regulation		Δνο		1.0mA≤ I <sub>O</sub> ≤40mA			85	mv
0 1 111 11			-20.7V>V <sub>I</sub> >-33	V, 1.0mA≤ l <sub>O</sub> ≤40mA	-17.1		-18.9	V
Output Voltage		Vo	$V_1 = -1.0V, 1.0mA \le I_0 \le 70mA$		-17.1		-18.9	
Quiescent Current			$T_J = +25^{\circ}C$				6.5	V mA mA
Quiescent Current	L	lα	T <sub>J</sub> = +125°C				6.0	
Quiescent	With Line		-21V≥V <sub>I</sub> ≥-33V				1.5	
Current Change	With Load	ΔlQ	1.0mA≤ I <sub>O</sub> ≤40n	nA			0.1	mA
Output Noise Volta	age	$V_N$	T <sub>A</sub> =+25°C,10H	lz≤f≤100KHz		150		μV
Ripple Rejection		RR	f = 120Hz, -23V≥V₁≥-33V T₁ = +25°C		33	48		dB
Dropout Voltage		V <sub>D</sub>	T <sub>J</sub> = +25°C			1.7		V

<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Change in V<sub>0</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# MC79L24A ELECTRICAL CHARACTERISTICS

 $(V_1 = -33V, I_0 = 40mA, C_1 = 0.33\mu F, C_0 = 0.1\mu F, 0^{\circ}C \le T_J \le + 125^{\circ}C$ , unless otherwise specified)

Charac	teristic	Symbol	Tes	t Conditions	Min	Тур	Max	Unit
Output Voltage		Vo	T <sub>J</sub> = +25°C		-23	-24	-25	V
Line Regulation			T 0500	-27V≥ V <sub>I</sub> ≥-38V			350	\/
		$\Delta V_{O}$	T <sub>J</sub> =+25°C	-28V≥ V <sub>I</sub> ≥-38V			300	mV
Load Regulation		4)/	T .0500	1.0mA≤ l <sub>O</sub> ≤100mA			200	
		ΔVO	$\Delta V_0$ $T_J = +25^{\circ}C$ $\frac{1.0 \text{m} \times 10^{\circ} \text{Total M}}{1.0 \text{m} A \leq 10^{\circ} \text{C}}$			100	mV	
Output Valtage	Output Voltage		V <sub>0</sub>		-22.8		-25.2	.,
Output voltage					-22.8		-25.2	V
	_		T <sub>J</sub> = +25°C				6.5	4
Quiescent Curren	t	lα	T <sub>.1</sub> = +125°C				6.0	mA
Quiescent	With Line	ΔΙο	-28V≥V <sub>I</sub> ≥-38V				1.5	
Current Change	With Load	ΔiQ	1.0mA≤ I <sub>O</sub> ≤40r	mA			0.1	mA
Output Noise Volt	age	V <sub>N</sub>	T <sub>A</sub> = +25°C,10Hz≤f≤100KHz			200		μV
Ripple Rejection		RR	f = 120Hz, -29\	f = 120Hz, -29V≥V₁≥-35V		47	_	dB
		IXIX	$T_J = +25^{\circ}C$		31	47		uБ
Dropout Voltage		V <sub>D</sub>	$T_J = +25^{\circ}C$			1.7		V

<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Change in V<sub>0</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.



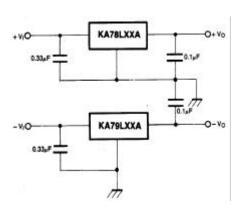
#### TYPICAL APPLICATIONS

#### **Design Considerations**

The MC79LXXA Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short-Circuit Protection that limits the maximum current the circuit will pass.

In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass

Fig. 1 Positive And Negative Regulator

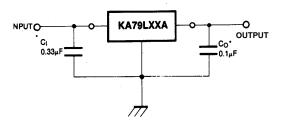


capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A  $0.33\mu F$  or larger tantalum,

mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The

bypass capacitor should be mounted with the shortest possible leads directly across the regulator's input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

Fig. 2 Typical Application



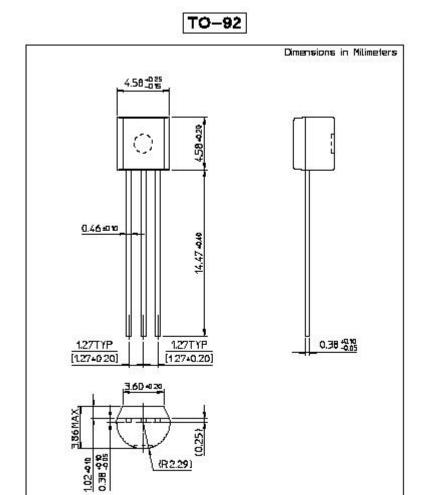
A common ground is required between the Input and the output voltages. The input voltage must remain typically 2.0V above the output voltage even during the low point on the input ripple voltage.

 $= C_1 \text{ is required} \quad \text{if regulator is located an} \\ \text{appreciable distance from power supply filter.} \\ ^** = C_0 \text{ improves stability and transient response.}$ 



SAMSUNG ELECTRONICS CO.,LTO.

# **PACKAGE DIMENSION**





# **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

 $E^2CMOS^{TM}$  PowerTrench® FACT Quiet Series QSTM QSTM

 $\begin{array}{lll} \mathsf{FAST}^{\circledR} & \mathsf{Quiet} \; \mathsf{Series^{\intercal M}} \\ \mathsf{FASTr^{\intercal M}} & \mathsf{SuperSOT^{\intercal M}\text{--}3} \\ \mathsf{GTO^{\intercal M}} & \mathsf{SuperSOT^{\intercal M}\text{--}6} \\ \mathsf{HiSeC^{\intercal M}} & \mathsf{SuperSOT^{\intercal M}\text{--}8} \\ \end{array}$ 

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

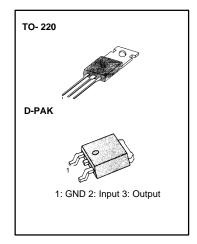
### PRODUCT STATUS DEFINITIONS

# **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

# **3-TERMINAL 0.5A NEGATIVE VOLTAGE REGULATORS**

The LM79MXX series of 3-Terminal medium current negative voltage regulators are monolithic integrated circuits designed as fixed voltage regulators. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially in destructible.



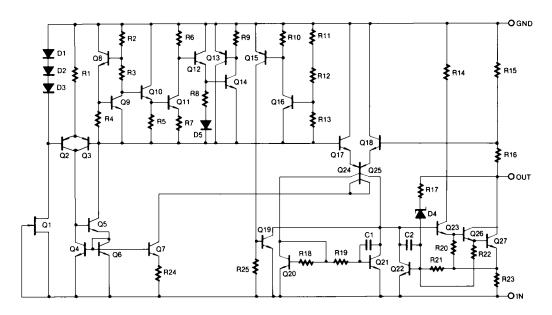
# **FEATURES**

- No external components required
- Output current in excess of 0.5A
- · Internal thermal-overload
- Internal short circuit current limiting
- Output transistor safe-area compensation
- Output Voltages of -5V, -6V,-8V,-12V,-15V,-18V and -24V

# **ORDERING INFORMATION**

Device	Package	Operating Temperature
LM79MXX	TO-220	0 ~ +125 °C
LM79MXXR	D-PAK	0 ~ +125 °C

# **SCHEMATHIC DIAGRAM**





# ABSOLUTE MAXIMUM RATINGS ( $T_A$ = +25 $^{\circ}$ C, unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage(for $V_O = -5V$ to -18V) (for $V_O = -24V$ )	V <sub>I</sub> V <sub>I</sub>	-35 -40	V V
Thermal Resistance Junction-Cases	R <sub>θJC</sub>	5	°C /W
Thermal Resistance Junction-Air	$R_{\theta JA}$	65	°C /W
Operating Temperature Range	$T_OPR$	0 ~ +125	°C
Storage Temperature Range	Тета	65 ~ +125	°C

# LM79MO5/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0  $^{\circ}$ C  $\leq$ T $_{J} \leq$  +125  $^{\circ}$ C, I $_{O}$  =350mA, V $_{I}$  =10V,unless otherwise specified, C $_{I}$  =0.33 $\mu$ F, C $_{O}$ =0.1 $\mu$ F)

Characteristic	Symbol	Test condition	MIN	TYP	MAX	Unit
		T <sub>J</sub> = +25 °C	-4.8	-5	-5.2	
Output Voltage	Vo	$I_0 = 5 \text{ to } 350\text{mA}$ $V_1 = -7 \text{ to } -25\text{V}$	-4.75	-5	-5.25	V
Line Regulation	$\Delta V_{O}$	$T_{J}$ = +25°C $V_{I}$ = -7 to -25V		7.0	50	mV
Line Regulation	Δνο	$V_{i} = +25 \text{ C}$ $V_{i} = -8 \text{ to } -25 \text{V}$		2.0	30	IIIV
Load Regulation	$\Delta V_{O}$	$I_O = 5mA$ to 500mA $T_J = 25$ °C		30	100	mV
Quiescent Current	lα	T <sub>J</sub> = 25 °C		3.0	6.0	mA
Quiescent Current		I <sub>O</sub> = 5 to 350mA			0.4	
Change	$\Delta I_Q$	$I_0 = 200 \text{mA}$ $V_1 = -8 \text{V to } -25 \text{V}$			0.4	mA
Output Voltage Drift	$\Delta V_{O}/\Delta T$	I <sub>O</sub> = 5mA		-0.2		mV/ °C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz, 100Khz T <sub>J</sub> = +25 °C		40		μV
Ripple Rejection	RR	f = 120Hz V <sub>i</sub> = -8 to -18V	54	60		dB
Dropout Voltage	$V_D$	$T_J = +25 ^{\circ}\text{C}, I_O = 500\text{mA}$		1.1		V
Short Circuit Current	I <sub>sc</sub>	T <sub>J</sub> = +25 °C, V <sub>I</sub> = -35V		140		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> = +25 °C		650		mA

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant junction temperature. Change in  $V_{O}$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.



# LM79MO6/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C  $\leq$ TJ  $\leq$  +125 °C, IO =350mA, VI = -11V, unless otherwise specified)

Characteristic	Symbol	Т	Test condition		Тур	Max	Unit
		T <sub>J</sub> = +25 °C	T,= +25 °C		- 6.0	- 6.25	
Output Voltage	Vo	$I_0 = 5 \text{ to } 350 \text{ r}$	<sub>O</sub> = 5 to 350mA				V
		$V_1 = -8.0 \text{ to } -2$	25V	- 5.7	- 6.0	- 6.3	
Line Regulation	$\Delta V_{\Omega}$	T <sub>J</sub> = +25 °C	$V_1 = -8 \text{ to } -25 \text{V}$		7.0	60	mV
Line Regulation	Δνο	I <sub>J</sub> = +25 °C	$V_1 = -9 \text{ to } -19V$		2.0	40	mv
Load Regulation	$\Delta V_{O}$	T <sub>J</sub> = +25 °C	$I_0 = 5.0 \text{mA} \text{ to } 500 \text{mA}$		30	120	mV
Quiescent Current	lα	T <sub>J</sub> = +25 °C			3	6	mA
Quiescent Current	Al	$I_0 = 5 \text{ to } 350 \text{ r}$	mA			0.4	
Change	$\Delta I_Q$	$V_1 = -8V \text{ to } -2$	5V			0.4	mA
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$			0.4		mV/ °C
Output Noise Voltage	$V_N$	f = 10Hz to 1	00KHz,T <sub>A</sub> = +25 °C		50		μV
Ripple Rejection	RR	f = 120Hz,Vi	= -9 to -19V	54	60		dB
Dropout Voltage	$V_D$	I <sub>O</sub> = 500mA, T <sub>J</sub> = +25 °C			1.1		V
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = -35V, T <sub>.J</sub> = +25 °C			140		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> = +25 °C			650		mA

<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Change in V<sub>0</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# LM79MO8/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0  $^{\circ}$ C  $\leq$ T<sub>J</sub>  $\leq$  +125  $^{\circ}$ C, I<sub>O</sub> =350mA, V<sub>I</sub> = -14V,unless otherwise specified)

Characteristic	Symbol	7	Test condition		Тур	Max	Unit	
		T <sub>J</sub> = +25 °C		- 7.7	- 8.0	- 8.3		
Output Voltage	Vo	$I_0 = 5 \text{ to } 350$	<sub>0</sub> = 5 to 350mA				V	
		$V_1 = -10.5 \text{ to}$	$V_1 = -10.5 \text{ to } -25 \text{V}$		- 8.0	- 8.4		
Line Degulation	41/	T .25.0C	$V_1 = -10.5 \text{ to } -25 \text{V}$		7.0	80	.,	
Line Regulation	$\Delta V_{O}$	T <sub>J</sub> = +25 °C	$V_1 = -11 \text{ to } -21 \text{V}$		2.0	50	mV	
Load Regulation	$\Delta V_{O}$	T <sub>J</sub> = +25 °C	I <sub>O</sub> = 5.0mA to 500mA		30	160	mV	
Quiescent Current	lα	T <sub>J</sub> = +25 °C			3	6	mA	
Quiescent Current	A I	$I_0 = 5 \text{ to } 350$	)mA			0.4	A	
Change	$\Delta I_Q$	$V_1 = -8V \text{ to } -2$	25V			0.4	mA	
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$			-0.6		mV/ °C	
Output Noise Voltage	$V_N$	f = 10Hz to 1	100KHz,T <sub>A</sub> = +25 °C		60		μV	
Ripple Rejection	RR	f = 120Hz,Vi	= -9 to -19V	54	59		dB	
Dropout Voltage	$V_D$	$I_0 = 500 \text{mA},$	I <sub>O</sub> = 500mA, T <sub>J</sub> = +25 °C		1.1		V	
Short Circuit Current	I <sub>sc</sub>	$V_1 = -35V, T_2$	J = +25 °C		140		mA	
Peak Current	$I_{PK}$	T <sub>J</sub> = +25 °C			650		mA	

<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.



# LM79M12/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0  $^{\circ}$ C  $\leq$ T $_{J} \leq$  +125  $^{\circ}$ C, I $_{O}$  =350mA, V $_{I}$  = -19V, unless otherwise specified)

Characteristic	Symbol	-	Test condition		Тур	Max	Unit
		T <sub>J</sub> = +25 °C		-11.5	-12	-12.5	
Output Voltage	Vo	$I_0 = 5 \text{ to } 350$	)mA				V
		$V_1 = -14.5 \text{ to}$	-30V	-11.4	-1.2	-12.6	
Line Regulation	$\Delta V_{\Omega}$	T - +25 °C	$V_1 = -14.5 \text{ to } -30V$ $V_1 = -15 \text{ to } -25V$		8.0	80	ma\/
	Δνο	IJ = +25 °C	$V_1 = -15 \text{ to } -25 \text{V}$		3.0	50	mV
Load Regulation	$\Delta V_{O}$	T <sub>J</sub> = +25°C	$I_0 = 5.0 \text{mA} \text{ to } 500 \text{mA}$		30	240	mV
Quiescent Current	lα	T <sub>J</sub> = +25 °C			3	6	mA
Quiescent Current	41	$I_0 = 5 \text{ to } 350$	)mA			0.4	
Change	$\Delta I_Q$	$V_1 = -14.5V$	to -30V			0.4	mA
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$			-0.8		mV/°C
Output Noise Voltage	$V_N$	f = 10Hz to	100KHz,T <sub>A</sub> =+25 °C		75		μV
Ripple Rejection	RR	f = 120Hz,V	<sub>I</sub> = -15 to -25V	54	60		dB
Dropout Voltage	V <sub>D</sub>	I <sub>O</sub> = 500mA, T <sub>J</sub> = +25 °C			1.1		V
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = -35V, T	V <sub>I</sub> = -35V, T <sub>.I</sub> = +25 °C		140		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> = +25 °C			650		mA

<sup>\*</sup>Load and line regulation are specified at constant junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# LM79M15/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C  $\leq$ T<sub>J</sub> $\leq$  +125 °C, I<sub>O</sub> =350mA, V<sub>I</sub> = -23V, unless otherwise specified)

Characteristic	Symbol	1	Test condition		Тур	Max	Unit
		T <sub>J</sub> = +25 °C		- 14.4	- 15	- 15.6	
Output Voltage	Vo	$I_0 = 5 \text{ to } 350$	I <sub>O</sub> = 5 to 350mA				V
		$V_1 = -17.5 \text{ to}$	-30V	- 14.25	- 15	- 15.75	
	41/	T .25 °C	$V_1 = -17.5 \text{ to } -30 \text{V}$ $V_2 = -18 \text{ to } -28 \text{V}$		9.0	80	mV
Line Regulation	$\Delta V_{O}$	T <sub>J</sub> = +25 °C	$V_1 = -18 \text{ to } -28 \text{V}$		5.0	50	111V
Load Regulation	$\Delta V_{O}$	T <sub>J</sub> = +25°C	I <sub>O</sub> = 5.0mA to 500mA		30	240	mV
Quiescent Current	ΙQ	T <sub>J</sub> = +25 °C	T <sub>.j</sub> = +25 °C		3	6	mA
Quiescent Current	Δlo	$I_0 = 5 \text{ to } 350$	)mA			0.4	A
Change	ΔiQ	$V_1 = -17.5V1$	to -28V			0.4	mA
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$			-1.0		mV/ °C
Output Noise Voltage	$V_N$	f = 10Hz to 1	100KHz,T <sub>A</sub> = +25 °C		90		μV
Ripple Rejection	RR	$f = 120Hz, V_1$	= -18.5 to -28.5V	54	59		dB
Dropout Voltage	$V_D$	$I_0 = 500 \text{mA},$	I <sub>O</sub> = 500mA, T <sub>J</sub> = +25 °C		1.1		V
Short Circuit Current	I <sub>sc</sub>	$V_1 = -35V, T_2$	V <sub>I</sub> = -35V, T <sub>.J</sub> = +25 °C		140		mA
Peak Current	$I_{PK}$	T <sub>J</sub> = +25 °C			650		mA

<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Change in V<sub>0</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.



# FIXED VOLTAGE REGULATOR(NEGATIVE)

# LM79M18/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤T<sub>J</sub>≤+125 °C, I<sub>O</sub> =350mA, V<sub>I</sub> = -27V, unless otherwise specified)

Characteristic	Symbol	Test condition	Min	Тур	Max	Unit
		T <sub>J</sub> = +25 °C	- 17.3	- 18	- 18.7	
Output Voltage	Vo	I <sub>O</sub> = 5 to 350mA				V
		$V_1 = -21 \text{ to } -33V$	- 17.1	- 18	- 18.9	
Line Degulation	$\Delta V_{O}$	$T_J = +25  ^{\circ}\text{C}$ $\frac{V_I = -21 \text{ to } -33\text{V}}{V_I = -24 \text{ to } -30\text{V}}$		9.0	80	mV
Line Regulation	Δνο	$V_1 = -24 \text{ to } -30 \text{V}$		5.0	80	IIIV
Load Regulation	$\Delta V_{O}$	$T_{J}$ = +25 °C $I_{O}$ = 5.0mA to 500mA		30	360	mV
Quiescent Current	lα	T <sub>J</sub> = +25 °C		3	6	mA
Quiescent Current	4.1	I <sub>O</sub> = 5 to 350mA			0.4	mA
Change	$\Delta I_Q$	$V_1 = -21V \text{ to } -33V$			0.4	MA
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_O = 5mA$		-1.0		mV/ °C
Output Noise Voltage	$V_N$	$f = 10Hz$ to $100KHz$ , $T_A = +25$ °C		110		μV
Ripple Rejection	RR	$f = 120Hz, V_1 = -22 \text{ to } -32V$	54	59		dB
Dropout Voltage	$V_D$	I <sub>O</sub> = 500mA, T <sub>J</sub> = +25 °C		1.1		V
Short Circuit Current	I <sub>sc</sub>	$V_{I} = -35V, T_{J} = +25  ^{\circ}C$		140		mA
Peak Current	$I_{PK}$	T <sub>J</sub> = +25 °C		650		mA

<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Change in V<sub>0</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# LM79M24/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤TJ≤+125 °C, IO =350mA, VI = - 33V, unless otherwise specified)

Characteristic	Symbol	Test condition	Min	Тур	Max	Unit
		T <sub>J</sub> = +25 °C	- 23	- 24	- 25	
Output Voltage	Vo	I <sub>O</sub> = 5 to 350mA				V
		$V_1 = -27 \text{ to } -38V$	- 22.8	- 24	- 25.2	
Line Regulation	$\Delta V_{\Omega}$	$T_J = +25  ^{\circ}\text{C}$ $\frac{V_1 = -27 \text{ to } -38 \text{V}}{V_1 = -30 \text{ to } -36 \text{V}}$		9.0	80	mV
	200	$V_1 = -30 \text{ to } -36V$		5.0	70	IIIV
Load Regulation	$\Delta V_{O}$	$T_{J}$ = +25 °C $I_{O}$ = 5.0mA to 500mA		30	300	mV
Quiescent Current	ΙQ	T <sub>J</sub> = +25 °C		3	6	mA
Quiescent Current		I <sub>O</sub> = 5 to 350mA			0.4	A
Change	$\Delta I_Q$	$V_1 = -27V \text{ to } -38V$			0.4	mA
Output Voltage Drift	$\Delta V_{O}/\Delta T$	I <sub>O</sub> = 5mA		-1.0		mV/ °C
Output Noise Voltage	$V_N$	f = 10Hz to 100KHz,T <sub>A</sub> = +25 °C		180		μV
Ripple Rejection	RR	$f = 120Hz, V_1 = -28 \text{ to } -38V$	54	58		dB
Dropout Voltage	$V_D$	I <sub>O</sub> = 500mA, T <sub>J</sub> = +25 °C		1.1		V
Short Circuit Current	I <sub>SC</sub>	V <sub>I</sub> = -35V, T <sub>J</sub> = +25 °C		140		mA
Peak Current	$I_{PK}$	T <sub>J</sub> = +25 °C		650		mA

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant junction temperature. Change in  $V_0$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.



#### **TYPICAL APPLICATIONS**

Bypass capacitors are recommended for stable operation of the KA79MXX series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors,  $(2\mu F)$  on the input,  $1\mu F$  on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electronics are used, their values should be  $10\mu F$  or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Fig. 1 Fixed Output Regulator

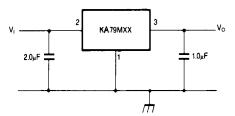
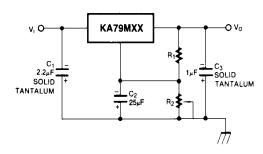


Fig. 2 Variable Output



#### Note

- 1. Required for stability. For value given, capacitor must be solid tantalum. 25μF aluminum electrolytic may be substituted
- 2.  $C_2$  improves transient response and ripple rejection. Do not increase beyond  $50\mu F$ .

$$V_{\text{OUT}} = V_{\text{SET}} \left( \frac{R_1 + R_2}{R_1} \right)$$

Select R<sub>2</sub> as follows

KA79M 05: 300Ω, KA79M12: 750Ω, KA79M15: 11Ω



# **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEX<sup>TM</sup> ISOPLANAR<sup>TM</sup> CoolFET<sup>TM</sup> MICROWIRE<sup>TM</sup>

CROSSVOLT<sup>TM</sup> POP<sup>TM</sup>

E<sup>2</sup>CMOS<sup>™</sup> PowerTrench<sup>™</sup>

FACT<sup>TM</sup> QS<sup>TM</sup>

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

 A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

### **PRODUCT STATUS DEFINITIONS**

#### **Definition of Terms**

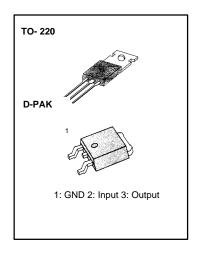
Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

#### 3-TERMINAL 0.5A NEGATIVE VOLTAGE REGULATORS

The KA79MXX series of 3-Terminal medium current negative voltage regulators are monolithic integrated circuits designed as fixed voltage regulators. These regulators employ internal current limiting, thermal shutdown and safe-area compensation making them essentially in destructible.

# **FEATURES**

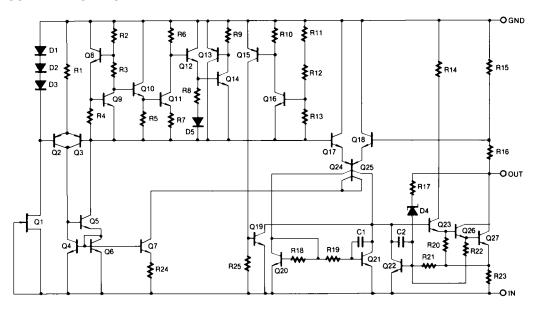
- No external components required
- Output current in excess of 0.5A
- Internal thermal-overload
- Internal short circuit current limiting
- Output transistor safe-area compensation
- Output Voltages of -5V, -6V,-8V,-12V,-15V,-18V and -24V



# **ORDERING INFORMATION**

Device	Package	Operating Temperature
KA79MXX	TO-220	0 ~ +125 °C
KA79MXXR	D-PAK	0 ~ +125 °C

# **SCHEMATHIC DIAGRAM**





Rev. C

# **ABSOLUTE MAXIMUM RATINGS** ( $T_A = +25 \, ^{\circ}\text{C}$ , unless otherwise specified)

Characteristic	Symbol	Value	Unit
Input Voltage(for V <sub>O</sub> = -5V to -18V)	Vı	-35	V
$(for V_0 = -24V)$	Vı	-40	V
Thermal Resistance Junction-Cases	$R_{\theta JC}$	5	°C /W
Thermal Resistance Junction-Air	$R_{\theta JA}$	65	°C /W
Operating Temperature Range	T <sub>OPR</sub>	0 ~ +125	°C
Storage Temperature Range	T <sub>STG</sub>	65 ~ +125	°C

# LM79MO5/R ELECTRICAL CHARACTERISTICS

 $(\text{Refer to test circuit, 0 } \circ \text{C} \leq \text{T}_{\text{J}} \leq +125 \, \circ \text{C}, \, \text{I}_{\text{O}} = 350 \text{mA}, \, \text{V}_{\text{I}} = 10 \text{V}, \\ \text{unless otherwise specified, C}_{\text{I}} = 0.33 \mu\text{F}, \, \text{C}_{\text{O}} = 0.1 \mu\text{F}) = 10 \, \text{V}, \\ \text{U} =$ 

Characteristic	Symbol	Test condition	MIN	TYP	MAX	Unit
		T <sub>J</sub> = +25 °C	-4.8	-5	-5.2	
Output Voltage	Vo	$I_0 = 5 \text{ to } 350\text{mA}$ $V_1 = -7 \text{ to } -25\text{V}$	-4.75	-5	-5.25	V
Line Regulation	$\Delta V_{O}$	$T_{J}=+25^{\circ}C$ $V_{I}=-7 \text{ to } -25V$		7.0	50	mV
Line Regulation	Δνο	$V_1 = -8 \text{ to } -25 \text{ V}$		2.0	30	IIIV
Load Regulation	ΔV <sub>O</sub>	$I_O = 5mA$ to 500mA $T_J = 25 ^{\circ}C$		30	100	mV
Quiescent Current	lα	T <sub>J</sub> = 25 °C		3.0	6.0	mA
Quiescent Current		I <sub>O</sub> = 5 to 350mA			0.4	
Change	$\Delta l_{Q}$	$I_0 = 200 \text{mA}$ $V_1 = -8 \text{V to } -25 \text{V}$			0.4	mA
Output Voltage Drift	$\Delta V_O/\Delta T$	I <sub>O</sub> = 5mA		-0.2		mV/ °C
Output Noise Voltage	V <sub>N</sub>	f = 10Hz, 100Khz T <sub>J</sub> = +25 °C		40		μV
Ripple Rejection	RR	f = 120Hz V <sub>i</sub> = -8 to -18V	54	60		dB
Dropout Voltage	$V_D$	$T_J = +25 ^{\circ}\text{C}, I_O = 500\text{mA}$		1.1		V
Short Circuit Current	I <sub>SC</sub>	T <sub>J</sub> = +25 °C, V <sub>I</sub> = -35V		140		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> = +25 °C		650		mA

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant junction temperature. Change in  $V_{O}$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.



# LM79MO6/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C  $\leq$ TJ  $\leq$  +125 °C, IO =350mA, VI = -11V, unless otherwise specified)

Characteristic	Symbol	Test condition		Min	Тур	Max	Unit
		T <sub>J</sub> = +25 °C		- 5.75	- 6.0	- 6.25	
Output Voltage	Vo	$I_0 = 5 \text{ to } 350 \text{ n}$	nA				V
		$V_1 = -8.0 \text{ to } -2$	5V	- 5.7	- 6.0	- 6.3	
Line Degulation	$\Delta V_{O}$	T <sub>.J</sub> = +25 °C	$V_1 = -8 \text{ to } -25 \text{V}$		7.0	60	mV
Line Regulation	Δνο	1 <sub>J</sub> = +25 °C	$V_1 = -9 \text{ to } -19V$		2.0	40	mv
Load Regulation	$\Delta V_{O}$	T <sub>J</sub> = +25 °C	I <sub>O</sub> = 5.0mA to 500mA		30	120	mV
Quiescent Current	ΙQ	T <sub>J</sub> = +25 °C			3	6	mA
Quiescent Current	4.1	$I_0 = 5 \text{ to } 350 \text{ n}$	nA			0.4	
Change	$\Delta I_Q$	$V_1 = -8V \text{ to } -28$	5V			0.4	mA
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_O = 5mA$			0.4		mV/ °C
Output Noise Voltage	$V_N$	f = 10Hz to 10	00KHz,T <sub>A</sub> = +25 °C		50		μV
Ripple Rejection	RR	f = 120Hz,Vi = -9 to -19V		54	60		dB
Dropout Voltage	$V_D$	I <sub>O</sub> = 500mA, T <sub>J</sub> = +25 °C			1.1		V
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = -35V, T <sub>J</sub> = +25 °C			140		mA
Peak Current	$I_{PK}$	T <sub>J</sub> = +25 °C	•		650		mA

<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Change in V<sub>0</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# LM79MO8/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C  $\leq$ T $_{J} \leq$  +125 °C, I $_{O}$  =350mA, V $_{I}$  = -14V,unless otherwise specified)

Characteristic	Symbol	Test condition		Min	Тур	Max	Unit
		T <sub>J</sub> = +25 °C		- 7.7	- 8.0	- 8.3	
Output Voltage	Vo	$I_0 = 5 \text{ to } 350$	mA				V
		$V_1 = -10.5 \text{ to}$	-25V	- 7.6	- 8.0	- 8.4	
Line Regulation	ΔVo	T₁= +25 °C	$V_1 = -10.5 \text{ to } -25 \text{V}$		7.0	80	\/
Line Regulation	Δνο	1 J= +25 °C	$V_1 = -11 \text{ to } -21 \text{V}$		2.0	50	mV
Load Regulation	$\Delta V_{O}$	T <sub>J</sub> = +25 °C	I <sub>O</sub> = 5.0mA to 500mA		30	160	mV
Quiescent Current	Ιq	T <sub>J</sub> = +25 °C			3	6	mA
Quiescent Current	$\Delta I_{\Omega}$	$I_0 = 5 \text{ to } 350$	mA			0.4	A
Change	ΔIQ	$V_1 = -8V \text{ to } -2$	25V			0.4	mA
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$			-0.6		mV/ °C
Output Noise Voltage	$V_N$	f = 10Hz to 1	100KHz,T <sub>A</sub> = +25 °C		60		μV
Ripple Rejection	RR	f = 120Hz,Vi = -9 to -19V		54	59		dB
Dropout Voltage	$V_D$	$I_0 = 500 \text{mA},$	T <sub>J</sub> = +25 °C		1.1		V
Short Circuit Current	Isc	$V_1 = -35V, T_2$	」= +25 °C		140		mA
Peak Current	$I_{PK}$	T <sub>J</sub> = +25 °C			650		mA

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant junction temperature. Change in V<sub>0</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.



# LM79M12/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0 °C ≤TJ≤+125 °C, IO =350mA, VI = - 19V, unless otherwise specified)

Characteristic	Symbol	Test condition	Min	Тур	Max	Unit
		T <sub>J</sub> = +25 °C	-11.5	-12	-12.5	
Output Voltage	Vo	I <sub>O</sub> = 5 to 350mA				V
		$V_1 = -14.5 \text{ to } -30 \text{V}$	-11.4	-1.2	-12.6	
Line Regulation	41/	$T_J = +25 ^{\circ}\text{C}$ $\frac{V_I = -14.5 \text{ to } -30\text{V}}{V_I = -15 \text{ to } -25\text{V}}$		8.0	80	\/
Line Regulation	$\Delta V_{O}$	$V_1 = -15 \text{ to } -25 \text{ V}$		3.0	50	mV
Load Regulation	$\Delta V_{O}$	$T_{J}$ = +25°C $I_{O}$ = 5.0mA to 500mA		30	240	mV
Quiescent Current	ΙQ	T <sub>J</sub> = +25 °C		3	6	mA
Quiescent Current	4.1	I <sub>O</sub> = 5 to 350mA			0.4	
Change	$\Delta I_Q$	$V_1 = -14.5V \text{ to } -30V$			0.4	mA
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$		-0.8		mV/°C
Output Noise Voltage	$V_N$	f = 10Hz to 100KHz,T <sub>A</sub> =+25 °C		75		μV
Ripple Rejection	RR	f = 120Hz,V <sub>I</sub> = -15 to -25V	54	60		dB
Dropout Voltage	$V_D$	I <sub>O</sub> = 500mA, T <sub>J</sub> = +25 °C		1.1		V
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = -35V, T <sub>J</sub> = +25 °C		140		mA
Peak Current	$I_{PK}$	T <sub>J</sub> = +25 °C		650		mA

<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Change in V<sub>O</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# LM79M15/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0  $^{\circ}$ C  $\leq$ T $_{J} \leq$  +125  $^{\circ}$ C, I $_{O}$  =350mA, V $_{I}$  = -23V, unless otherwise specified)

Characteristic	Symbol	7	Test condition	Min	Тур	Max	Unit
		T <sub>J</sub> = +25 °C		- 14.4	- 15	- 15.6	
Output Voltage	Vo	$I_0 = 5 \text{ to } 350$	)mA				V
		$V_1 = -17.5$ to	-30V	- 14.25	- 15	- 15.75	
Line Demoleties	$\Delta V_{O}$	T _ 125 °C	$V_1 = -17.5 \text{ to } -30V$ $V_1 = -18 \text{ to } -28V$		9.0	80	m\/
Line Regulation	Δν0	1J=+25 C	$V_1 = -18 \text{ to } -28 \text{V}$		5.0	50	mV ~-
Load Regulation	$\Delta V_{O}$	T <sub>J</sub> = +25°C	$I_0 = 5.0 \text{mA} \text{ to } 500 \text{mA}$		30	240	mV
Quiescent Current	Ιq	T <sub>J</sub> = +25 °C			3	6	mA
Quiescent Current	Δlo	$I_0 = 5 \text{ to } 350$	)mA			0.4	A
Change	ΔiQ	$V_I = -17.5V t$	to -28V			0.4	mA
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_0 = 5mA$			-1.0		mV/ °C
Output Noise Voltage	$V_N$	f = 10Hz to 1	100KHz,T <sub>A</sub> = +25 °C		90		μV
Ripple Rejection	RR	$f = 120Hz, V_1$	= -18.5 to -28.5V	54	59		dB
Dropout Voltage	$V_D$	$I_0 = 500 \text{mA},$	T <sub>J</sub> = +25 °C		1.1		V
Short Circuit Current	I <sub>sc</sub>	$V_1 = -35V, T_2$	J = +25 °C		140		mA
Peak Current	$I_{PK}$	T <sub>J</sub> = +25 °C			650		mA

 $<sup>^{\</sup>star}$  Load and line regulation are specified at constant junction temperature. Change in  $V_0$  due to heating effects must be taken into account separately. Pulse testing with low duty is used.



# LM79M18/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0  $^{\circ}$ C  $\leq$ T<sub>J</sub> $\leq$ +125  $^{\circ}$ C, I<sub>O</sub> =350mA, V<sub>I</sub> = -27V, unless otherwise specified)

Characteristic	Symbol	Test condition	Min	Тур	Max	Unit
		T <sub>J</sub> = +25 °C	- 17.3	- 18	- 18.7	
Output Voltage	Vo	I <sub>O</sub> = 5 to 350mA				V
		V <sub>I</sub> = -21 to -33V	- 17.1	- 18	- 18.9	
Line Degulation	$\Delta V_{O}$	$T_J = +25  ^{\circ}\text{C}$ $\frac{V_I = -21 \text{ to } -33\text{V}}{V_I = -24 \text{ to } -30\text{V}}$		9.0	80	mV
Line Regulation	ΔVO	$V_1 = -24 \text{ to } -30 \text{V}$		5.0	80	IIIV
Load Regulation	$\Delta V_{O}$	$T_{J}$ = +25 °C $I_{O}$ = 5.0mA to 500mA		30	360	mV
Quiescent Current	lα	T <sub>J</sub> = +25 °C		3	6	mA
Quiescent Current	4.1	I <sub>O</sub> = 5 to 350mA			0.4	mA
Change	$\Delta I_Q$	$V_1 = -21V \text{ to } -33V$			0.4	MA
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_O = 5mA$		-1.0		mV/ °C
Output Noise Voltage	$V_N$	f = 10Hz to 100KHz,T <sub>A</sub> = +25 °C		110		μV
Ripple Rejection	RR	$f = 120Hz, V_1 = -22 \text{ to } -32V$	54	59		dB
Dropout Voltage	$V_D$	I <sub>O</sub> = 500mA, T <sub>J</sub> = +25 °C		1.1		V
Short Circuit Current	I <sub>sc</sub>	V <sub>I</sub> = -35V, T <sub>J</sub> = +25 °C		140		mA
Peak Current	$I_{PK}$	T <sub>J</sub> = +25 °C		650		mA

<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Change in V<sub>0</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.

# LM79M24/R ELECTRICAL CHARACTERISTICS

(Refer to test circuit, 0  $^{\circ}$ C  $\leq$ T $_{J} \leq$  +125  $^{\circ}$ C, I $_{O}$  =350mA, V $_{I}$  = - 33V, unless otherwise specified)

Characteristic	Symbol	Test condition	Min	Тур	Max	Unit
		T <sub>J</sub> = +25 °C	- 23	- 24	- 25	
Output Voltage	Vo	I <sub>O</sub> = 5 to 350mA				V
		$V_1 = -27 \text{ to } -38V$	- 22.8	- 24	- 25.2	
Line Regulation	$\Delta V_{O}$	$V_1 = -27 \text{ to } -38 \text{V}$		9.0	80	mV
Line Regulation	ΔVO	$T_J = +25  ^{\circ}C  \frac{V_I = -27 \text{ to } -38V}{V_I = -30 \text{ to } -36V}$		5.0	70	mv
Load Regulation	$\Delta V_{O}$	$T_J$ = +25 °C $I_O$ = 5.0mA to 500	mA	30	300	mV
Quiescent Current	Ιq	T <sub>J</sub> = +25 °C		3	6	mA
Quiescent Current	4.1	I <sub>O</sub> = 5 to 350mA			0.4	A
Change	$\Delta I_Q$	$V_1 = -27V \text{ to } -38V$			0.4	mA
Output Voltage Drift	$\Delta V_{O}/\Delta T$	$I_O = 5mA$		-1.0		mV/ °C
Output Noise Voltage	$V_N$	$f = 10Hz$ to $100KHz$ , $T_A = +25$ $^{\circ}$	С	180		μV
Ripple Rejection	RR	$f = 120Hz, V_1 = -28 \text{ to } -38V$	54	58		dB
Dropout Voltage	$V_D$	$I_{O} = 500$ mA, $T_{J} = +25$ °C		1.1		<b>V</b>
Short Circuit Current	I <sub>SC</sub>	$V_{I} = -35V, T_{J} = +25  ^{\circ}C$		140		mA
Peak Current	I <sub>PK</sub>	T <sub>J</sub> = +25 °C		650		mA

<sup>\*</sup> Load and line regulation are specified at constant junction temperature. Change in V<sub>0</sub> due to heating effects must be taken into account separately. Pulse testing with low duty is used.



# **TYPICAL APPLICATIONS**

Bypass capacitors are recommended for stable operation of the KA79MXX series of regulators over the input voltage and output current ranges. Output bypass capacitors will improve the transient response of the regulator.

The bypass capacitors,  $(2\mu F$  on the input,  $1\mu F$  on the output) should be ceramic or solid tantalum which have good high frequency characteristics. If aluminum electronics are used, their values should be  $10\mu F$  or larger. The bypass capacitors should be mounted with the shortest leads, and if possible, directly across the regulator terminals.

Fig. 1 Fixed Output Regulator

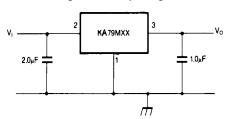
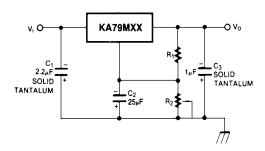


Fig. 2 Variable Output



#### Note

- 1. Required for stability. For value given, capacitor must be solid tantalum. 25µF aluminum electrolytic may be substituted.
- 2.  $C_2$  improves transient response and ripple rejection. Do not increase beyond  $50\mu F$ .

$$V_{OUT} = V_{SET} \left( \frac{R_1 + R_2}{R_1} \right)$$

Select R<sub>2</sub> as follows

KA79M 05: 300 $\Omega$ , KA79M12: 750 $\Omega$ , KA79M15: 11 $\Omega$ 



# **TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

 $E^2CMOS^{TM}$  PowerTrench® FACT Quiet Series QSTM QSTM

 $\begin{array}{lll} \mathsf{FAST}^{\circledR} & \mathsf{Quiet} \; \mathsf{Series^{\intercal M}} \\ \mathsf{FASTr^{\intercal M}} & \mathsf{SuperSOT^{\intercal M}\text{--}3} \\ \mathsf{GTO^{\intercal M}} & \mathsf{SuperSOT^{\intercal M}\text{--}6} \\ \mathsf{HiSeC^{\intercal M}} & \mathsf{SuperSOT^{\intercal M}\text{--}8} \\ \end{array}$ 

#### **DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

#### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

### PRODUCT STATUS DEFINITIONS

# **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.